

# High Performance Architectures

Basic Concepts and Taxonomy

# Basic computational models

- Turing
- von Neumann (and many extensions)
- Dataflow
- ...

# Key features of basic computational models

Computational model	Turing	von Neumann	Object-based	Dataflow	Applicative	Predicate logic-based
<b>Basic items of computation</b>	Elements of the tape symbol set Mappings defined on them	Data assigned to named entities (variables) Operations performed on data	Objects, which can be manipulated by a set of messages Messages sent to manipulate objects	Data assigned to named entities (variables) Operations performed on data	Arguments Applications of functions to their arguments	Elements of sets Predicates declared to them
<b>Style</b>	Procedural			Declarative		
<b>Problem description model</b>	<p>Input data</p>	<p>Input data</p>	<p>Initial states of objects</p>	<p>Input data</p>	<p>Arguments of the functions to be evaluated</p>	<p>Goal statement</p>
<b>Interpretation of how to perform the computation</b>	Starting with the initial state, a sequence of subsequent states will be performed until a final state is reached	The given sequence of instructions will be executed using the input data	The given sequence of messages will be executed	Input data flows through the dataflow graph and, as a consequence, output data is produced	The function with the given arguments is subsequently rewritten by substituting the function definitions referenced and performing the possible reductions until no more substitutions or reductions are feasible	The goal statement is subsequently rewritten using resolution until a logical inference is found or no more unifications are possible
<b>Assumed execution model</b>	<b>Execution semantics</b> State transition semantics	<b>Execution semantics</b> State transition semantics	<b>Execution semantics</b> State transition semantics	<b>Execution semantics</b> Dataflow semantics	<b>Execution semantics</b> Reduction semantics	<b>Execution semantics</b> SLD-resolution
<b>Control of the execution sequence</b>	Control driven	Control driven	Control driven	Data driven (eager evaluation)	Demand driven (lazy evaluation)	Defined by both the goal processing rule and search rule
<b>Concurrency</b>	Sequential			Parallel		

# The von Neumann computational model

- Basic items of computation are **data**
  - variables (named data entities)
  - memory or register locations whose addresses correspond to the names of the variables
  - data container
  - multiple assignments of data to variables are allowed
- Problem description model is **procedural** (sequence of instructions)
- Execution model is state transition semantics
  - Finite State Machine

# von Neumann model vs. finite state machine

– As far as execution is concerned the von Neumann model behaves like a finite state machine (FSM)

- $FSM = \{ I, G, \delta, G_0, G_f \}$
- $I$ : the input alphabet, given as the set of the instructions
- $G$ : the set of the state (global), data state space  $D$ , control state space  $C$ , flags state space  $F$ ,  $G = D \times C \times F$
- $\delta$ : the transition function:  $\delta: I \times G \rightarrow G$
- $G_0$ : the initial state
- $G_f$ : the final state

# Key characteristics of

## the von Neumann model

- Consequences of multiple assignments of data
  - history sensitive
  - side effects
- Consequences of control-driven execution
  - computation is basically a sequential one
- ++ easily be implemented
- Related language
  - allow declaration of variables with multiple assignments
  - provide a proper set of control statements to implement the control-driven mode of execution

# Extensions of the von Neumann computational model

- new abstraction of parallel execution
- communication mechanism allows the transfer of data between executable units
  - unprotected shared (global) variables
  - shared variables protected by modules or monitors
  - message passing, and
  - rendezvous
- synchronization mechanism
  - semaphores
  - signals
  - events
  - queues
  - barrier synchronization

# Instruction-Level Parallel Processors

{**Objective**: executing two or more instructions in parallel}

Improve CPU performance by:

- increasing clock rates
  - (CPU running at 2GHz!)
- increasing the number of instructions to be executed in parallel
  - (executing 6 instructions at the same time)



# How do we increase the number of instructions to be executed?

Traditional  
von Neumann processors

Scalar  
ILP-processors

Superscalar  
ILP-processors

(Sequential issue,  
sequential execution)

(Sequential issue,  
parallel execution)

(Parallel issue,  
parallel execution)



Parallelism of instruction execution



Parallelism of instruction issue

*Typical  
implementation*

*Non-pipelined  
processors*

*Processors with multiple  
non-pipelined EUs and  
pipelined processors*

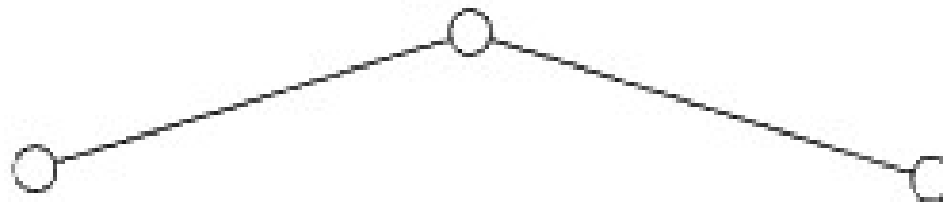
*VLIW and superscalar  
processors embodying  
multiple pipelined EUs*



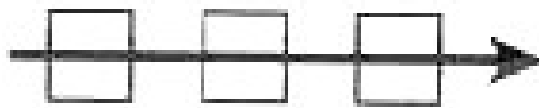
Processor performance

# Time and Space parallelism

Internal of operation  
principle  
of ILP-processors



**Pipelined operation**

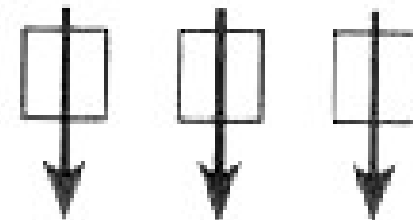


$EU_1$   $EU_2$   $EU_m$

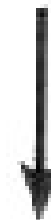


**Pipelined processors**

**Parallel operation**

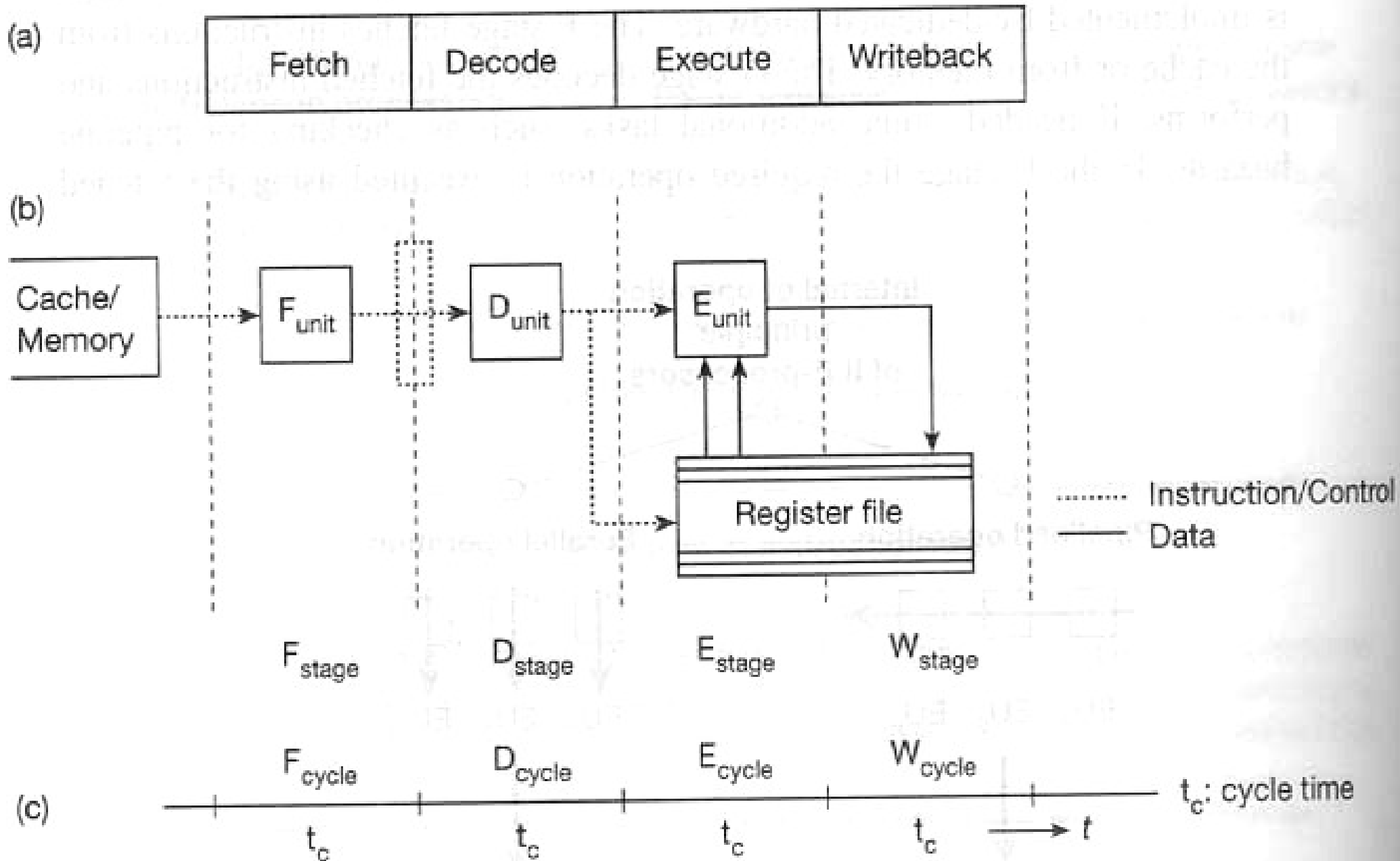


$EU_1$   $EU_2$   $EU_m$



**VLIW and superscalar processors**

# Pipeline (assembly line)

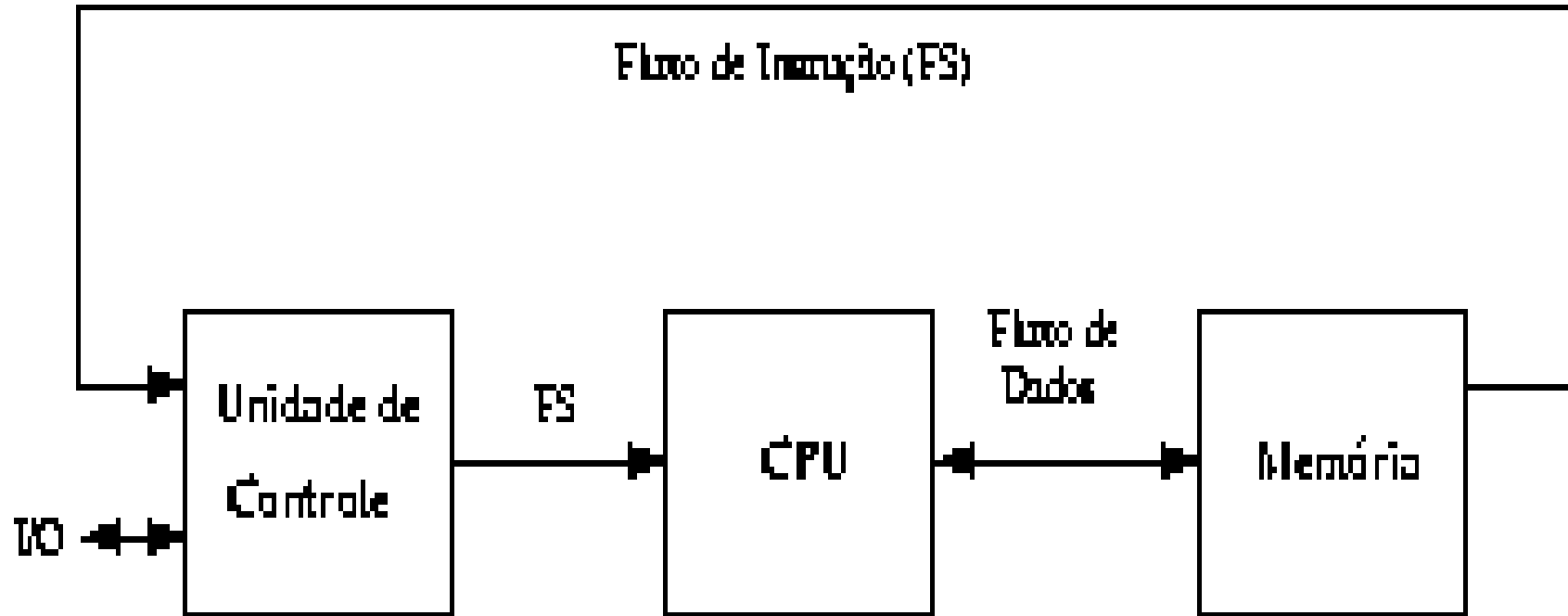




# Flynn's Taxonomy

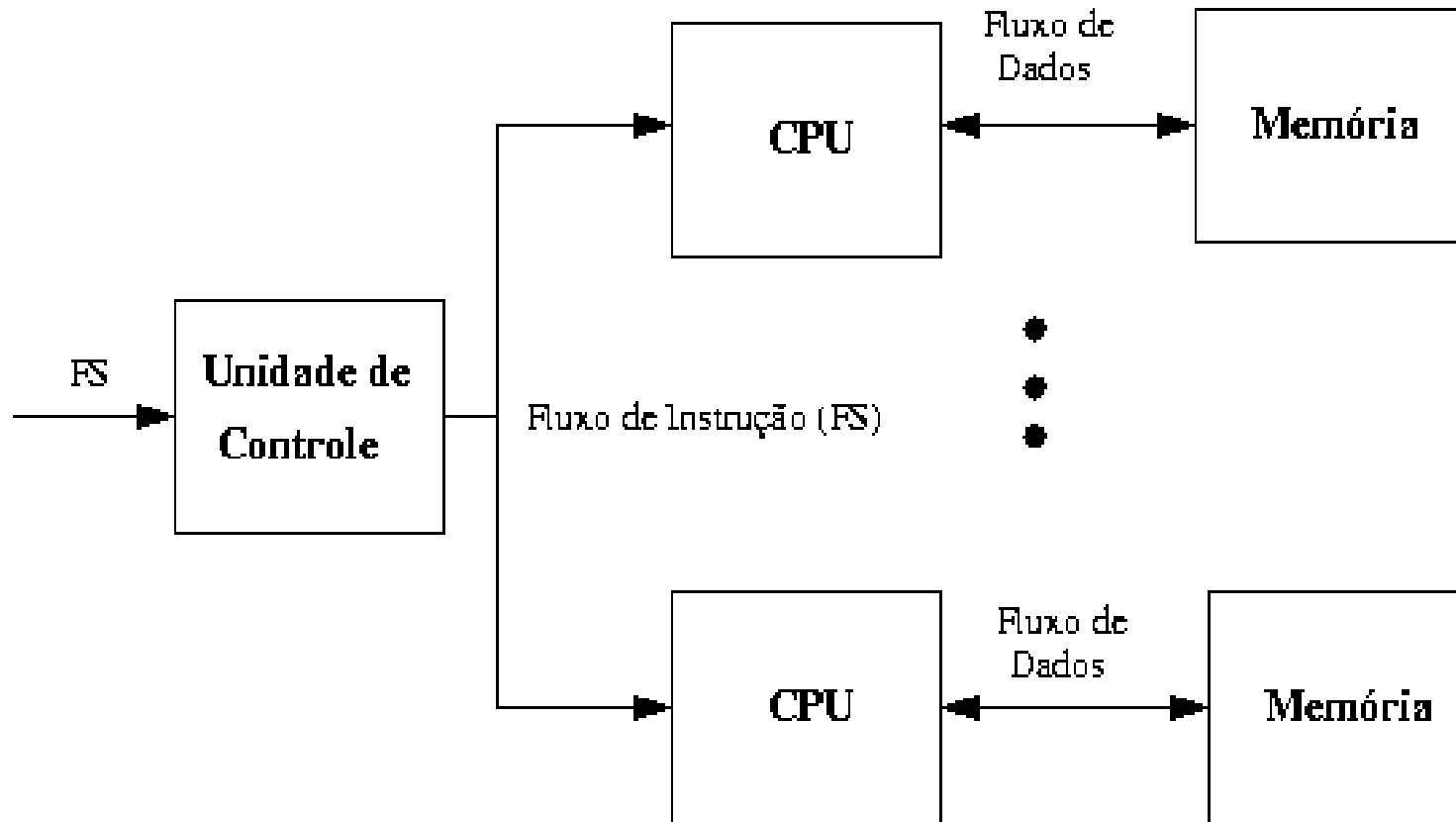
- Organizes the processor architectures according to the data and instruction stream
  - SISD - *Single Instruction, Single Data stream*
  - SIMD - *Single Instruction, Multiple Data stream*
  - MISD - *Multiple instruction, Single Data stream*
  - MIMD - *Multiple Instruction, Multiple Data stream*

# SISD



**Exemplos: Estações de trabalho e Computadores pessoais com um único processador**

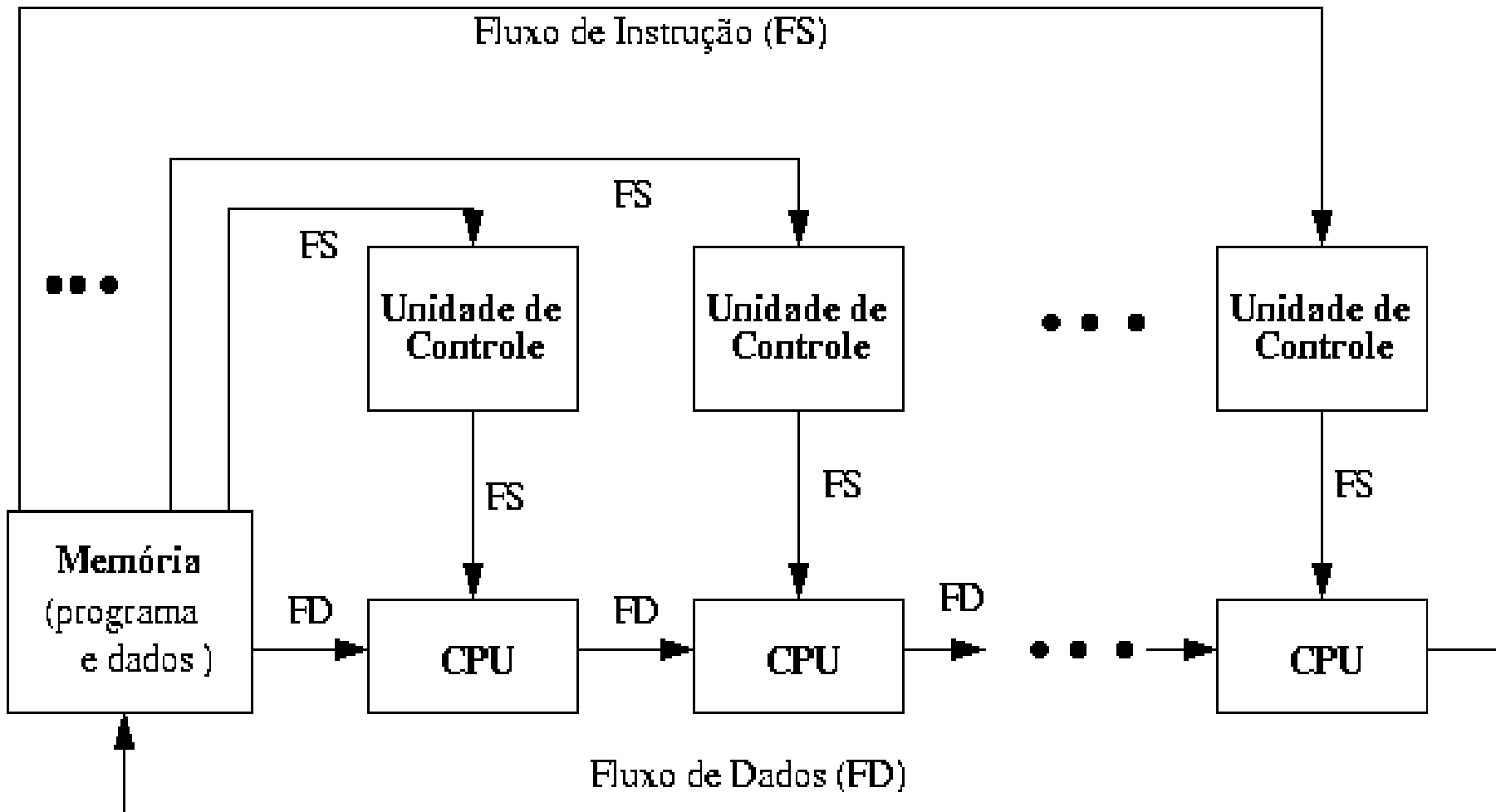
# SIMD



**Exemplos: ILIAC IV, MPP, DHP, MASP MP-2 e CPU Vetoriais**

**Extensões multimídia são consideradas como uma forma de paralelismo SIMD**

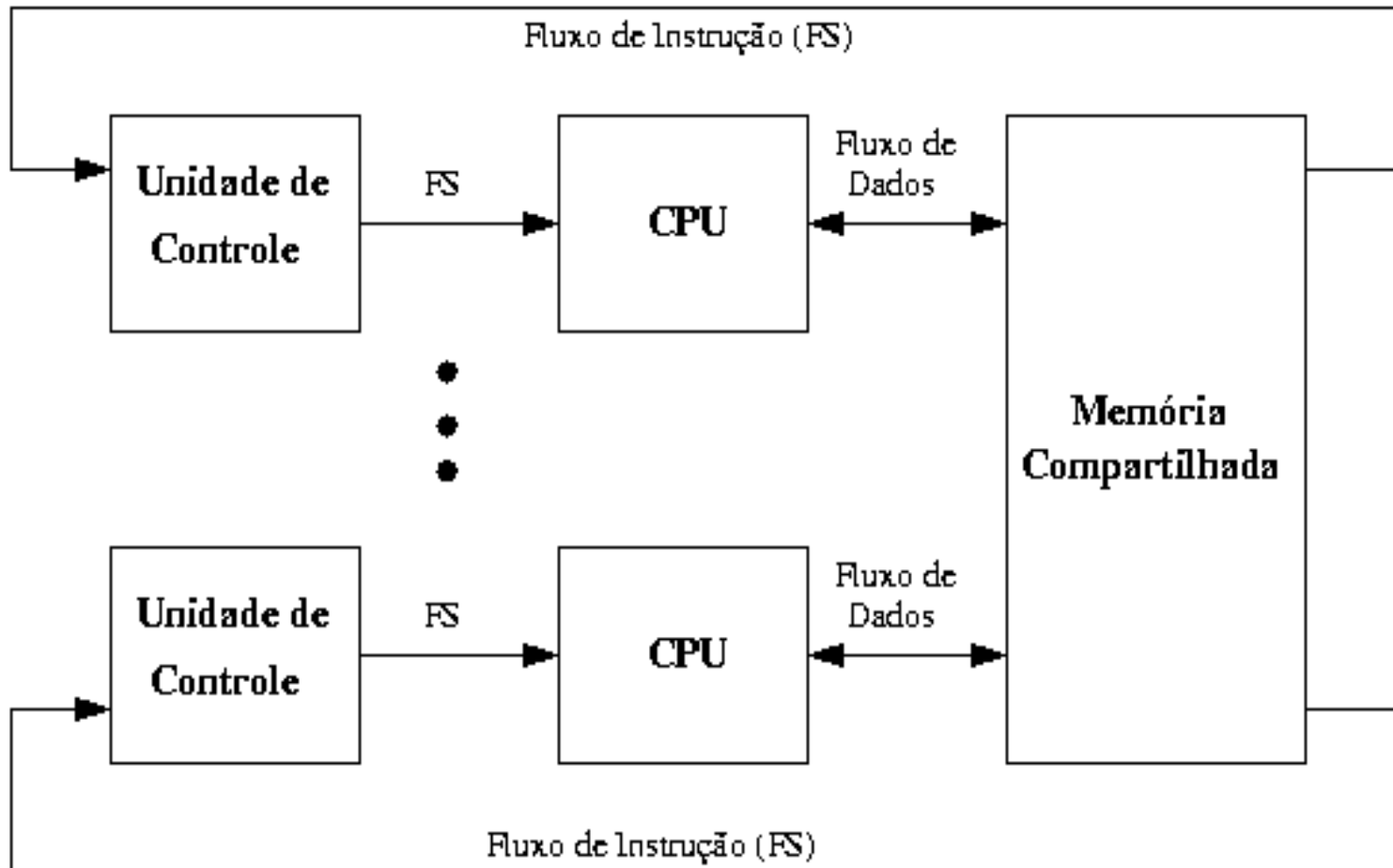
# MISD



**Exemplos: Arrays Sistólicos**



# MIMD



**Exemplos: Cosmic Cube,  
nCube 2, iPSC, FX-2000,  
SGI Origin, Sun Enterprise  
5000 e Redes de  
Computadores**

**Mais difundida  
Memória Compartilhada  
Memória Distribuída**

**Flexível**

***Usa microprocessadores off-the-shelf***

# Resume

OBS.: The Flynn's taxonomy is a reference model. Actually, there exist some processors using features of more than one category. There are many Taxonomy proposals for Parallel Architectures. See R. Duncan's paper!

- MIMD

- Most of the parallel machines
- It seems adequate to the general purpose parallel computing

- SIMD

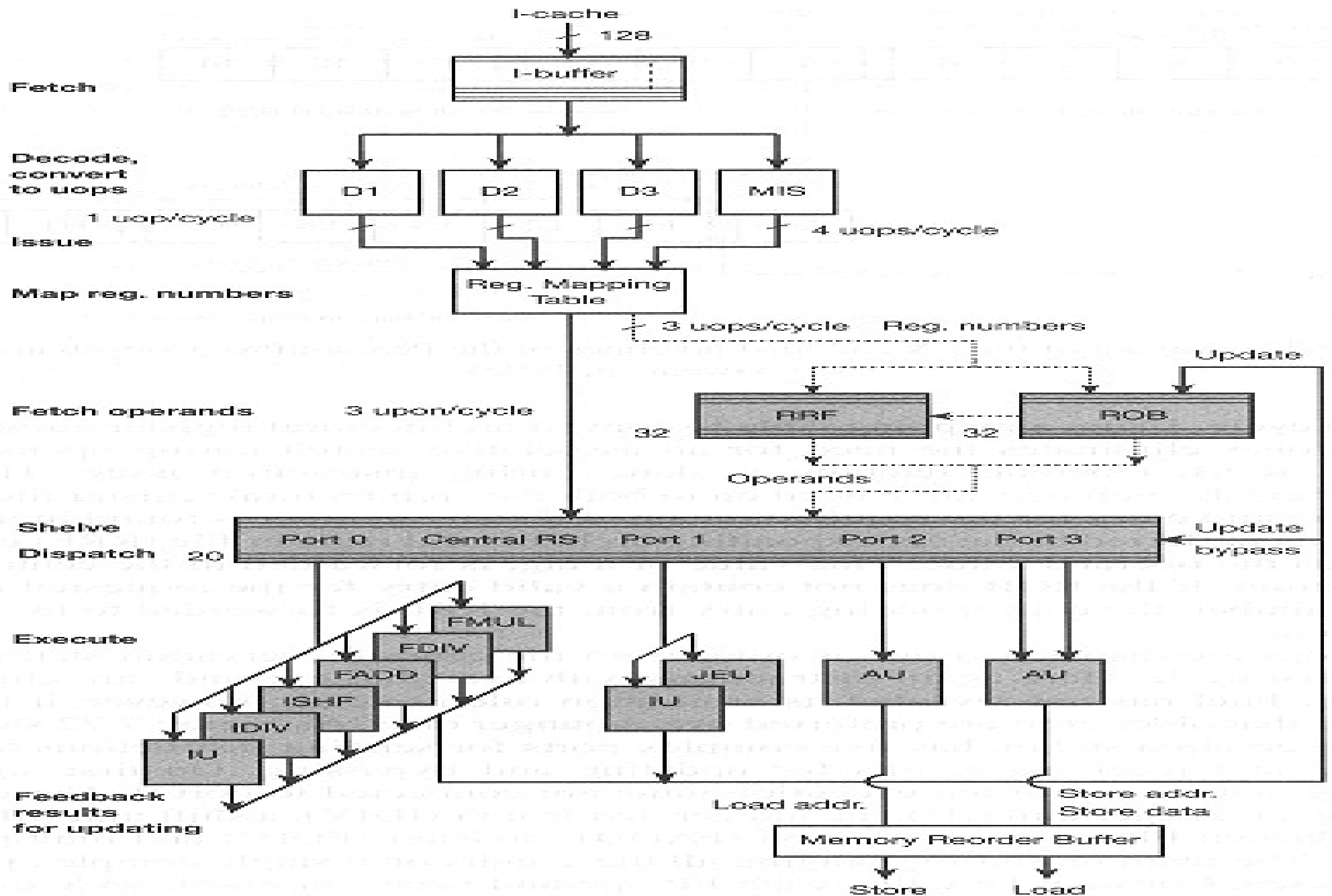
- MISD

- SISD

- Sequential computing

# Case Studies: PentiumPro

## Core part of the micro-architecture



# PentiumPro Long pipeline: Layout of the FX and load pipelines

