

MicroBlaze Processor Reference Guide

*Embedded Development Kit
EDK 9.2i*

UG081 (v8.0)



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MicroBlaze Processor Reference Guide UG081 (v8.0)

The following table shows the revision history for this document.

Date	Version	Revision
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About This Guide

The MicroBlaze™ Processor Reference Guide provides information about the 32-bit soft processor, MicroBlaze, which is part of the Embedded Processor Development Kit (EDK). The document is intended as a guide to the MicroBlaze hardware architecture.

Guide Contents

This guide contains the following chapters:

- Chapter 1, “[MicroBlaze Architecture](#)”, contains an overview of MicroBlaze features as well as information on Big-Endian bit-reversed format, 32-bit general purpose registers, cache software support, and Fast Simplex Link interfaces.
- Chapter 2, “[MicroBlaze Signal Interface Description](#)”, describes the types of signal interfaces that can be used to connect MicroBlaze.
- Chapter 3, “[MicroBlaze Application Binary Interface](#)”, describes the Application Binary Interface important for developing software in assembly language for the soft processor.
- Chapter 4, “[MicroBlaze Instruction Set Architecture](#)”, provides notation, formats, and instructions for the Instruction Set Architecture of MicroBlaze.

For additional information, go to <http://support.xilinx.com>. The following table lists some of the resources you can access directly using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx® design flows, from design entry to verification and debugging. http://support.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records. http://support.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches. http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Application+Notes
Data Book	Pages from <i>The Programmable Logic Data Book</i> , which contains device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging. http://support.xilinx.com/xlnx/xweb/xil_publications_index.jsp
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues. http://support.xilinx.com/support/troubleshoot/psolvers.htm

Resource	Description/URL
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment. http://www.support.xilinx.com/xlnx/xil_tt_home.jsp
GNU Manuals	The entire set of GNU manuals. http://www.gnu.org/manual

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Courier font	Messages, prompts, and program files that the system displays.	<code>speed grade: - 100</code>
Courier bold	Literal commands that you enter in a syntactical statement.	ngdbuild <i>design_name</i>
Helvetica bold	Commands that you select from a menu.	File → Open
	Keyboard shortcuts	Ctrl+C
Italic font	Variables in a syntax statement for which you must supply values.	ngdbuild <i>design_name</i>
	References to other manuals.	See the <i>Development System Reference Guide</i> for more information.
	Emphasis in text.	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected.
Square brackets []	An optional entry or parameter. However, in bus specifications, such as bus [7:0] , they are required.	ngdbuild [<i>option_name</i>] <i>design_name</i>
Braces { }	A list of items from which you must choose one or more.	lowpwr = {on off}
Vertical bar	Separates items in a list of choices.	lowpwr = {on off}

Convention	Meaning or Use	Example
Vertical ellipsis · · ·	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' · · ·
Horizontal ellipsis ...	Repetitive material that has been omitted	allow block <i>block_name</i> <i>loc1 loc2 ... locn;</i>

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section “ Additional Resources ” for details. Refer to “ Title Formats ” in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the <i>Virtex-II Handbook</i> .
Blue, underlined text	Hyperlink to a web-site (URL)	Go to http://www.xilinx.com for the latest speed files.

MicroBlaze Architecture

This chapter contains an overview of MicroBlaze™ features and detailed information on MicroBlaze architecture including Big-Endian bit-reversed format, 32-bit general purpose registers, virtual-memory management, cache software support, and Fast Simplex Link (FSL) interfaces.

This chapter has the following sections:

- “Overview”
- “Data Types and Endianness”
- “Instructions”
- “Registers”
- “Pipeline Architecture”
- “Memory Architecture”
- “Privileged Instructions”
- “Virtual-Memory Management”
- “Reset, Interrupts, Exceptions, and Break”
- “Instruction Cache”
- “Data Cache”
- “Floating Point Unit (FPU)”
- “Fast Simplex Link (FSL)”
- “Debug and Trace”

Overview

The MicroBlaze™ embedded processor soft core is a reduced instruction set computer (RISC) optimized for implementation in Xilinx® Field Programmable Gate Arrays (FPGAs). Figure 1-1 shows a functional block diagram of the MicroBlaze core.

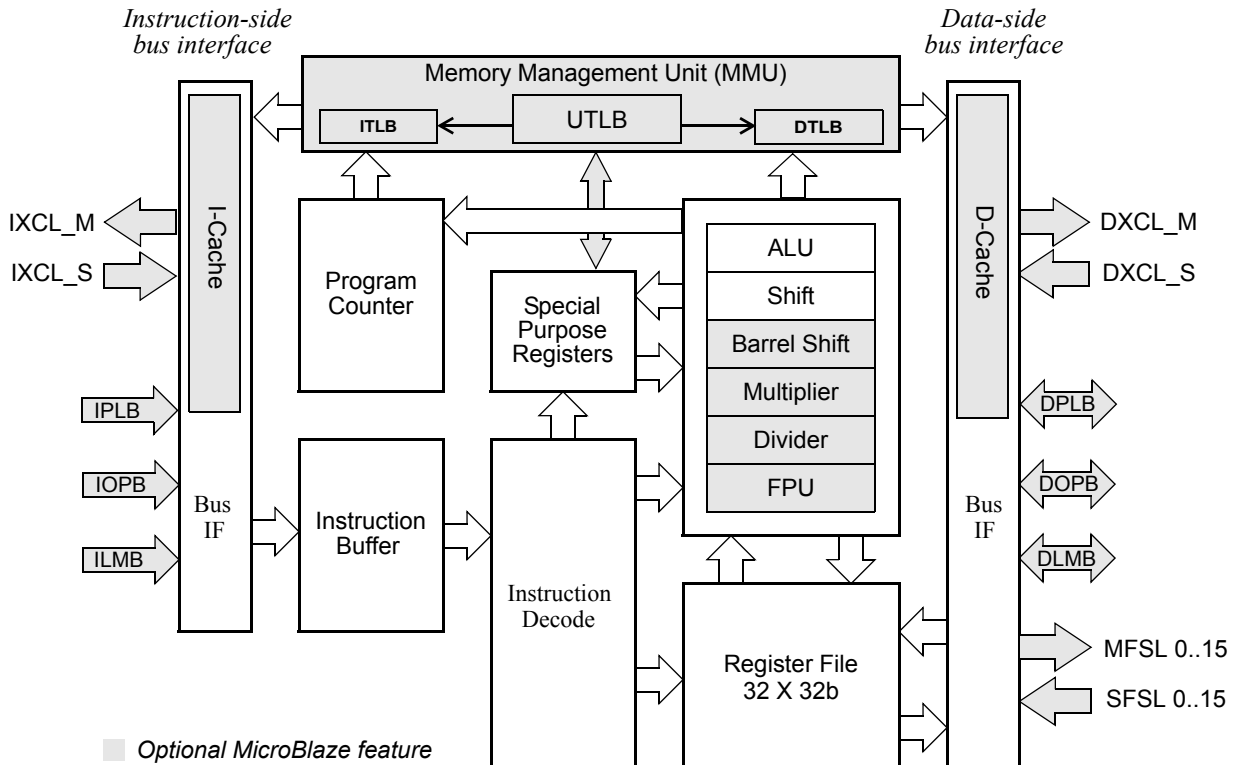


Figure 1-1: MicroBlaze Core Block Diagram

Features

The MicroBlaze soft core processor is highly configurable, allowing you to select a specific set of features required by your design.

The fixed feature set of the processor includes:

- Thirty-two 32-bit general purpose registers
- 32-bit instruction word with three operands and two addressing modes
- 32-bit address bus
- Single issue pipeline

In addition to these fixed features, the MicroBlaze processor is parameterized to allow selective enabling of additional functionality. Older (deprecated) versions of MicroBlaze support a subset of the optional features described in this manual. Only the latest (preferred) version of MicroBlaze (v7.00) supports all options.

Xilinx recommends that all new designs use the latest **preferred** version of the MicroBlaze processor.

Table 1-1, page 11 provides an overview of the configurable features by Microblaze versions.

Table 1-1: Configurable Feature Overview by MicroBlaze Version

Feature	MicroBlaze Versions			
	v4.00	v5.00	v6.00	v7.00
Version Status	deprecated	deprecated	deprecated	preferred
Processor pipeline depth	3	5	3/5	3/5
On-chip Peripheral Bus (OPB) data side interface	option	option	option	option
On-chip Peripheral Bus (OPB) instruction side interface	option	option	option	option
Local Memory Bus (LMB) data side interface	option	option	option	option
Local Memory Bus (LMB) instruction side interface	option	option	option	option
Hardware barrel shifter	option	option	option	option
Hardware divider	option	option	option	option
Hardware debug logic	option	option	option	option
Fast Simplex Link (FSL) interfaces	0-7	0-7	0-7	0-15
Machine status set and clear instructions	option	Yes	option	option
Instruction cache over IOPB interface	option	No	No	No
Data cache over IOPB interface	option	No	No	No
Instruction cache over CacheLink (IXCL) interface	option	option	option	option
Data cache over CacheLink (DXCL) interface	option	option	option	option
4 or 8-word cache line on XCL	4	option	option	option
Hardware exception support	option	option	option	option
Pattern compare instructions	option	Yes	option	option
Floating point unit (FPU)	option	option	option	option
Disable hardware multiplier ¹		option	option	option
Hardware debug readable ESR and EAR	Yes	Yes	Yes	Yes
Processor Version Register (PVR)	-	option	option	option
Area or speed optimized	-	-	option	option
Hardware multiplier 64-bit result	-	-	option	option
LUT cache memory	-	-	option	option
Processor Local Bus (PLB) data side interface	-	-	-	option
Processor Local Bus (PLB) instruction side interface	-	-	-	option
Floating point conversion and square root instructions	-	-	-	option
Memory Management Unit (MMU)	-	-	-	option
Extended Fast Simplex Link (FSL) instructions	-	-	-	option

1. Used in Virtex™-II and subsequent families, for saving MUL18 and DSP48 primitives.

Data Types and Endianness

MicroBlaze uses Big-Endian bit-reversed format to represent data. The hardware supported data types for MicroBlaze are word, half word, and byte. The bit and byte organization for each type is shown in the following tables.

Table 1-2: Word Data Type

Byte address	n	n+1	n+2	n+3
Byte label	0	1	2	3
Byte significance	MSByte			LSByte
Bit label	0			31
Bit significance	MSBit			LSBit

Table 1-3: Half Word Data Type

Byte address	n	n+1
Byte label	0	1
Byte significance	MSByte	LSByte
Bit label	0	15
Bit significance	MSBit	LSBit

Table 1-4: Byte Data Type

Byte address	n	
Bit label	0	7
Bit significance	MSBit	LSBit

Instructions

All MicroBlaze instructions are 32 bits and are defined as either Type A or Type B. Type A instructions have up to two source register operands and one destination register operand. Type B instructions have one source register and a 16-bit immediate operand (which can be extended to 32 bits by preceding the Type B instruction with an imm instruction). Type B instructions have a single destination register operand. Instructions are provided in the following functional categories: arithmetic, logical, branch, load/store, and special. Table 1-6 lists the MicroBlaze instruction set. Refer to Chapter 4, “MicroBlaze Instruction Set Architecture” for more information on these instructions. Table 1-5 describes the instruction set nomenclature used in the semantics of each instruction.

Table 1-5: Instruction Set Nomenclature

Symbol	Description
Ra	R0 - R31, General Purpose Register, source operand a
Rb	R0 - R31, General Purpose Register, source operand b
Rd	R0 - R31, General Purpose Register, destination operand
SPR[x]	Special Purpose Register number x
MSR	Machine Status Register = SPR[1]
ESR	Exception Status Register = SPR[5]
EAR	Exception Address Register = SPR[3]
FSR	Floating Point Unit Status Register = SPR[7]
PVR x	Processor Version Register, where x is the register number = SPR[8192 + x]
BTR	Branch Target Register = SPR[11]
PC	Execute stage Program Counter = SPR[0]
$x[y]$	Bit y of register x
$x[y:z]$	Bit range y to z of register x
\bar{x}	Bit inverted value of register x
Imm	16 bit immediate value
Imm x	x bit immediate value
FSL x	4 bit Fast Simplex Link (FSL) port designator where x is the port number
C	Carry flag, MSR[29]
Sa	Special Purpose Register, source operand
Sd	Special Purpose Register, destination operand
s(x)	Sign extend argument x to 32-bit value
*Addr	Memory contents at location Addr (data-size aligned)
:=	Assignment operator
=	Equality comparison

Table 1-5: Instruction Set Nomenclature (Continued)

Symbol	Description
!=	Inequality comparison
>	Greater than comparison
>=	Greater than or equal comparison
<	Less than comparison
<=	Less than or equal comparison
+	Arithmetic add
*	Arithmetic multiply
/	Arithmetic divide
>> <i>x</i>	Bit shift right <i>x</i> bits
<< <i>x</i>	Bit shift left <i>x</i> bits
and	Logic AND
or	Logic OR
xor	Logic exclusive OR
op1 if cond else op2	Perform <i>op1</i> if condition <i>cond</i> is true, else perform <i>op2</i>
&	Concatenate. E.g. “0000100 & Imm7” is the concatenation of the fixed field “0000100” and a 7 bit immediate value.
signed	Operation performed on signed integer data type. All arithmetic operations are performed on signed word operands, unless otherwise specified
unsigned	Operation performed on unsigned integer data type
float	Operation performed on floating point data type

Table 1-6: MicroBlaze Instruction Set Summary

Type A	0-5	6-10	11-15	16-20	21-31	Semantics
Type B	0-5	6-10	11-15	16-31		
ADD Rd,Ra,Rb	000000	Rd	Ra	Rb	0000000000	$Rd := Rb + Ra$
RSUB Rd,Ra,Rb	000001	Rd	Ra	Rb	0000000000	$Rd := Rb + \overline{Ra} + 1$
ADDC Rd,Ra,Rb	000010	Rd	Ra	Rb	0000000000	$Rd := Rb + Ra + C$
RSUBC Rd,Ra,Rb	000011	Rd	Ra	Rb	0000000000	$Rd := Rb + \overline{Ra} + C$
ADDK Rd,Ra,Rb	000100	Rd	Ra	Rb	0000000000	$Rd := Rb + Ra$
RSUBK Rd,Ra,Rb	000101	Rd	Ra	Rb	0000000000	$Rd := Rb + \overline{Ra} + 1$
ADDKC Rd,Ra,Rb	000110	Rd	Ra	Rb	0000000000	$Rd := Rb + Ra + C$
RSUBKC Rd,Ra,Rb	000111	Rd	Ra	Rb	0000000000	$Rd := Rb + \overline{Ra} + C$

Table 1-6: MicroBlaze Instruction Set Summary (Continued)

Type A	0-5	6-10	11-15	16-20	21-31	Semantics
Type B	0-5	6-10	11-15	16-31		
CMP Rd,Ra,Rb	000101	Rd	Ra	Rb	00000000001	$Rd := Rb + \overline{Ra} + 1$ Rd[0] := 0 if (Rb >= Ra) else Rd[0] := 1
CMPU Rd,Ra,Rb	000101	Rd	Ra	Rb	00000000011	$Rd := Rb + \overline{Ra} + 1$ (unsigned) Rd[0] := 0 if (Rb >= Ra, unsigned) else Rd[0] := 1
ADDI Rd,Ra,Imm	001000	Rd	Ra	Imm		$Rd := s(Imm) + Ra$
RSUBI Rd,Ra,Imm	001001	Rd	Ra	Imm		$Rd := s(Imm) + \overline{Ra} + 1$
ADDIC Rd,Ra,Imm	001010	Rd	Ra	Imm		$Rd := s(Imm) + Ra + C$
RSUBIC Rd,Ra,Imm	001011	Rd	Ra	Imm		$Rd := s(Imm) + \overline{Ra} + C$
ADDIK Rd,Ra,Imm	001100	Rd	Ra	Imm		$Rd := s(Imm) + Ra$
RSUBIK Rd,Ra,Imm	001101	Rd	Ra	Imm		$Rd := s(Imm) + \overline{Ra} + 1$
ADDIKC Rd,Ra,Imm	001110	Rd	Ra	Imm		$Rd := s(Imm) + Ra + C$
RSUBIKC Rd,Ra,Imm	001111	Rd	Ra	Imm		$Rd := s(Imm) + \overline{Ra} + C$
MUL Rd,Ra,Rb	010000	Rd	Ra	Rb	00000000000	$Rd := Ra * Rb$
MULH Rd,Ra,Rb	010000	Rd	Ra	Rb	00000000001	$Rd := (Ra * Rb) \gg 32$ (signed)
MULHU Rd,Ra,Rb	010000	Rd	Ra	Rb	00000000011	$Rd := (Ra * Rb) \gg 32$ (unsigned)
MULHSU Rd,Ra,Rb	010000	Rd	Ra	Rb	00000000010	$Rd := (Ra, \text{signed} * Rb, \text{unsigned}) \gg 32$ (signed)
BSRA Rd,Ra,Rb	010001	Rd	Ra	Rb	01000000000	$Rd := s(Ra \gg Rb)$
BSLL Rd,Ra,Rb	010001	Rd	Ra	Rb	10000000000	$Rd := (Ra \ll Rb) \& 0$
MULI Rd,Ra,Imm	011000	Rd	Ra	Imm		$Rd := Ra * s(Imm)$
BSRLI Rd,Ra,Imm	011001	Rd	Ra	0000000000 & Imm5		$Rd := 0 \& (Ra \gg Imm5)$
BSRAI Rd,Ra,Imm	011001	Rd	Ra	00000010000 & Imm5		$Rd := s(Ra \gg Imm5)$
BSLLI Rd,Ra,Imm	011001	Rd	Ra	00000100000 & Imm5		$Rd := (Ra \ll Imm5) \& 0$
IDIV Rd,Ra,Rb	010010	Rd	Ra	Rb	00000000000	$Rd := Rb/Ra$
IDIVU Rd,Ra,Rb	010010	Rd	Ra	Rb	00000000010	$Rd := Rb/Ra$, unsigned
TNEAGETD Rd,Rb	010011	Rd	00000	Rb	0NOTAE 00000	$Rd := \text{FSL } Rb[28:31]$ (data read) MSR[FSL] := 1 if (FSL_S_Control = 1) MSR[C] := not FSL_S_Exists if N = 1
TNAPUTD Ra,Rb	010011	00000	Ra	Rb	0NOTA0 00000	$\text{FSL } Rb[28:31] := Ra$ (data write) MSR[C] := FSL_M_Full if N = 1

Table 1-6: MicroBlaze Instruction Set Summary (Continued)

Type A	0-5	6-10	11-15	16-20	21-31	Semantics
Type B	0-5	6-10	11-15	16-31		
<i>TNECAGETD</i> Rd,Rb	010011	Rd	00000	Rb	0N1TAE 00000	Rd := FSL Rb[28:31] (control read) MSR[FSL] := 1 if (FSL_S_Control = 0) MSR[C] := not FSL_S_Exists if N = 1
<i>TNCAPUTD</i> Ra,Rb	010011	00000	Ra	Rb	0N1T40 00000	FSL Rb[28:31] := Ra (control write) MSR[C] := FSL_M_Full if N = 1
FADD Rd,Ra,Rb	010110	Rd	Ra	Rb	0000000000	Rd := Rb+Ra, float ¹
FRSUB Rd,Ra,Rb	010110	Rd	Ra	Rb	0001000000	Rd := Rb-Ra, float ¹
FMUL Rd,Ra,Rb	010110	Rd	Ra	Rb	0010000000	Rd := Rb*Ra, float ¹
FDIV Rd,Ra,Rb	010110	Rd	Ra	Rb	0011000000	Rd := Rb/Ra, float ¹
FCMP.UN Rd,Ra,Rb	010110	Rd	Ra	Rb	0100000000	Rd := 1 if (Rb = NaN or Ra = NaN, float ¹) else Rd := 0
FCMP.LT Rd,Ra,Rb	010110	Rd	Ra	Rb	0100001000	Rd := 1 if (Rb < Ra, float ¹) else Rd := 0
FCMP.EQ Rd,Ra,Rb	010110	Rd	Ra	Rb	0100010000	Rd := 1 if (Rb = Ra, float ¹) else Rd := 0
FCMP.LE Rd,Ra,Rb	010110	Rd	Ra	Rb	0100011000	Rd := 1 if (Rb <= Ra, float ¹) else Rd := 0
FCMP.GT Rd,Ra,Rb	010110	Rd	Ra	Rb	0100100000	Rd := 1 if (Rb > Ra, float ¹) else Rd := 0
FCMP.NE Rd,Ra,Rb	010110	Rd	Ra	Rb	0100101000	Rd := 1 if (Rb != Ra, float ¹) else Rd := 0
FCMP.GE Rd,Ra,Rb	010110	Rd	Ra	Rb	0100110000	Rd := 1 if (Rb >= Ra, float ¹) else Rd := 0
FLT Rd,Ra	010110	Rd	Ra	0	0101000000	Rd := float (Ra) ¹
FINT Rd,Ra	010110	Rd	Ra	0	0110000000	Rd := int (Ra) ¹
FSQRT Rd,Ra	010110	Rd	Ra	0	0111000000	Rd := sqrt (Ra) ¹
<i>TNEAGET</i> Rd,FSLx	011011	Rd	00000	0N0TAE000000 & FSLx		Rd := FSLx (data read, blocking if N = 0) MSR[FSL] := 1 if (FSLx_S_Control = 1) MSR[C] := not FSLx_S_Exists if N = 1
<i>TNAPUT</i> Ra,FSLx	011011	00000	Ra	1N0T40000000 & FSLx		FSLx := Ra (data write, blocking if N = 0) MSR[C] := FSLx_M_Full if N = 1
<i>TNECAGET</i> Rd,FSLx	011011	Rd	00000	0N1TAE000000 & FSLx		Rd := FSLx (control read, blocking if N = 0) MSR[FSL] := 1 if (FSLx_S_Control = 0) MSR[C] := not FSLx_S_Exists if N = 1
<i>TNCAPUT</i> Ra,FSLx	011011	00000	Ra	1N1T40000000 & FSLx		FSLx := Ra (control write, blocking if N = 0) MSR[C] := FSLx_M_Full if N = 1

Table 1-6: MicroBlaze Instruction Set Summary (Continued)

Type A	0-5	6-10	11-15	16-20	21-31	Semantics
Type B	0-5	6-10	11-15	16-31		
OR Rd,Ra,Rb	100000	Rd	Ra	Rb	00000000000	Rd := Ra or Rb
AND Rd,Ra,Rb	100001	Rd	Ra	Rb	00000000000	Rd := Ra and Rb
XOR Rd,Ra,Rb	100010	Rd	Ra	Rb	00000000000	Rd := Ra xor Rb
ANDN Rd,Ra,Rb	100011	Rd	Ra	Rb	00000000000	Rd := Ra and \overline{Rb}
PCMPBF Rd,Ra,Rb	100000	Rd	Ra	Rb	10000000000	Rd := 1 if (Rb[0:7] = Ra[0:7]) else Rd := 2 if (Rb[8:15] = Ra[8:15]) else Rd := 3 if (Rb[16:23] = Ra[16:23]) else Rd := 4 if (Rb[24:31] = Ra[24:31]) else Rd := 0
PCMPEQ Rd,Ra,Rb	100010	Rd	Ra	Rb	10000000000	Rd := 1 if (Rd = Ra) else Rd := 0
PCMPNE Rd,Ra,Rb	100011	Rd	Ra	Rb	10000000000	Rd := 1 if (Rd != Ra) else Rd := 0
SRA Rd,Ra	100100	Rd	Ra	0000000000000001		Rd := s(Ra >> 1) C := Ra[31]
SRC Rd,Ra	100100	Rd	Ra	0000000000100001		Rd := C & (Ra >> 1) C := Ra[31]
SRL Rd,Ra	100100	Rd	Ra	0000000000100001		Rd := 0 & (Ra >> 1) C := Ra[31]
SEXT8 Rd,Ra	100100	Rd	Ra	0000000001100000		Rd := s(Ra[24:31])
SEXT16 Rd,Ra	100100	Rd	Ra	0000000001100001		Rd := s(Ra[16:31])
WIC Ra,Rb	100100	00000	Ra	Rb	01101000	ICache_Line[Ra >> 4].Tag := 0 if (C_ICACHE_LINE_LEN = 4) ICache_Line[Ra >> 5].Tag := 0 if (C_ICACHE_LINE_LEN = 8)
WDC Ra,Rb	100100	00000	Ra	Rb	01100100	DCache_Line[Ra >> 4].Tag := 0 if (C_DCACHE_LINE_LEN = 4) DCache_Line[Ra >> 5].Tag := 0 if (C_DCACHE_LINE_LEN = 8)
MTS Sd,Ra	100101	00000	Ra	11 & Sd		SPR[Sd] := Ra, where: <ul style="list-style-type: none"> • SPR[0x0001] is MSR • SPR[0x0007] is FSR • SPR[0x1000] is PID • SPR[0x1001] is ZPR • SPR[0x1002] is TLBX • SPR[0x1003] is TLBLO • SPR[0x1004] is TLBHI • SPR[0x1005] is TLBSX

Table 1-6: MicroBlaze Instruction Set Summary (Continued)

Type A	0-5	6-10	11-15	16-20	21-31	Semantics
Type B	0-5	6-10	11-15	16-31		
MFS Rd,Sa	100101	Rd	00000	10 & Sa		Rd := SPR[<i>Sa</i>], where: <ul style="list-style-type: none"> • SPR[0x0000] is PC • SPR[0x0001] is MSR • SPR[0x0003] is EAR • SPR[0x0005] is ESR • SPR[0x0007] is FSR • SPR[0x000B] is BTR • SPR[0x000D] is EDR • SPR[0x1000] is PID • SPR[0x1001] is ZPR • SPR[0x1002] is TLBX • SPR[0x1003] is TLBLO • SPR[0x1004] is TLBHI • SPR[0x2000 to 0x200B] is PVR[0 to 11]
MSRCLR Rd,Imm	100101	Rd	00001	00 & Imm14		Rd := MSR MSR := MSR and $\overline{\text{Imm14}}$
MSRSET Rd,Imm	100101	Rd	00000	00 & Imm14		Rd := MSR MSR := MSR or Imm14
BR Rb	100110	00000	00000	Rb	0000000000	PC := PC + Rb
BRD Rb	100110	00000	10000	Rb	0000000000	PC := PC + Rb
BRLD Rd,Rb	100110	Rd	10100	Rb	0000000000	PC := PC + Rb Rd := PC
BRA Rb	100110	00000	01000	Rb	0000000000	PC := Rb
BRAD Rb	100110	00000	11000	Rb	0000000000	PC := Rb
BRALD Rd,Rb	100110	Rd	11100	Rb	0000000000	PC := Rb Rd := PC
BRK Rd,Rb	100110	Rd	01100	Rb	0000000000	PC := Rb Rd := PC MSR[BIP] := 1
BEQ Ra,Rb	100111	00000	Ra	Rb	0000000000	PC := PC + Rb if Ra = 0
BNE Ra,Rb	100111	00001	Ra	Rb	0000000000	PC := PC + Rb if Ra != 0
BLT Ra,Rb	100111	00010	Ra	Rb	0000000000	PC := PC + Rb if Ra < 0
BLE Ra,Rb	100111	00011	Ra	Rb	0000000000	PC := PC + Rb if Ra <= 0
BGT Ra,Rb	100111	00100	Ra	Rb	0000000000	PC := PC + Rb if Ra > 0
BGE Ra,Rb	100111	00101	Ra	Rb	0000000000	PC := PC + Rb if Ra >= 0
BEQD Ra,Rb	100111	10000	Ra	Rb	0000000000	PC := PC + Rb if Ra = 0

Table 1-6: MicroBlaze Instruction Set Summary (Continued)

Type A	0-5	6-10	11-15	16-20	21-31	Semantics
Type B	0-5	6-10	11-15	16-31		
BNED Ra,Rb	100111	10001	Ra	Rb	0000000000	PC := PC + Rb if Ra != 0
BLTD Ra,Rb	100111	10010	Ra	Rb	0000000000	PC := PC + Rb if Ra < 0
BLED Ra,Rb	100111	10011	Ra	Rb	0000000000	PC := PC + Rb if Ra <= 0
BGTD Ra,Rb	100111	10100	Ra	Rb	0000000000	PC := PC + Rb if Ra > 0
BGED Ra,Rb	100111	10101	Ra	Rb	0000000000	PC := PC + Rb if Ra >= 0
ORI Rd,Ra,Imm	101000	Rd	Ra	Imm		Rd := Ra or s(Imm)
ANDI Rd,Ra,Imm	101001	Rd	Ra	Imm		Rd := Ra and s(Imm)
XORI Rd,Ra,Imm	101010	Rd	Ra	Imm		Rd := Ra xor s(Imm)
ANDNI Rd,Ra,Imm	101011	Rd	Ra	Imm		Rd := Ra and $\overline{s(Imm)}$
IMM Imm	101100	00000	00000	Imm		Imm[0:15] := Imm
RTSD Ra,Imm	101101	10000	Ra	Imm		PC := Ra + s(Imm)
RTID Ra,Imm	101101	10001	Ra	Imm		PC := Ra + s(Imm) MSR[IE] := 1
RTBD Ra,Imm	101101	10010	Ra	Imm		PC := Ra + s(Imm) MSR[BIP] := 0
RTED Ra,Imm	101101	10100	Ra	Imm		PC := Ra + s(Imm) MSR[EE] := 1, MSR[EIP] := 0 ESR := 0
BRI Imm	101110	00000	00000	Imm		PC := PC + s(Imm)
BRID Imm	101110	00000	10000	Imm		PC := PC + s(Imm)
BRLID Rd,Imm	101110	Rd	10100	Imm		PC := PC + s(Imm) Rd := PC
BRAI Imm	101110	00000	01000	Imm		PC := s(Imm)
BRAID Imm	101110	00000	11000	Imm		PC := s(Imm)
BRALID Rd,Imm	101110	Rd	11100	Imm		PC := s(Imm) Rd := PC
BRKI Rd,Imm	101110	Rd	01100	Imm		PC := s(Imm) Rd := PC MSR[BIP] := 1
BEQI Ra,Imm	101111	00000	Ra	Imm		PC := PC + s(Imm) if Ra = 0
BNEI Ra,Imm	101111	00001	Ra	Imm		PC := PC + s(Imm) if Ra != 0
BLTI Ra,Imm	101111	00010	Ra	Imm		PC := PC + s(Imm) if Ra < 0
BLEI Ra,Imm	101111	00011	Ra	Imm		PC := PC + s(Imm) if Ra <= 0
BGTI Ra,Imm	101111	00100	Ra	Imm		PC := PC + s(Imm) if Ra > 0

Table 1-6: MicroBlaze Instruction Set Summary (Continued)

Type A	0-5	6-10	11-15	16-20	21-31	Semantics
Type B	0-5	6-10	11-15	16-31		
BGEI Ra,Imm	101111	00101	Ra	Imm		$PC := PC + s(Imm)$ if $Ra \geq 0$
BEQID Ra,Imm	101111	10000	Ra	Imm		$PC := PC + s(Imm)$ if $Ra = 0$
BNEID Ra,Imm	101111	10001	Ra	Imm		$PC := PC + s(Imm)$ if $Ra \neq 0$
BLTID Ra,Imm	101111	10010	Ra	Imm		$PC := PC + s(Imm)$ if $Ra < 0$
BLEID Ra,Imm	101111	10011	Ra	Imm		$PC := PC + s(Imm)$ if $Ra \leq 0$
BGTID Ra,Imm	101111	10100	Ra	Imm		$PC := PC + s(Imm)$ if $Ra > 0$
BGEID Ra,Imm	101111	10101	Ra	Imm		$PC := PC + s(Imm)$ if $Ra \geq 0$
LBU Rd,Ra,Rb	110000	Rd	Ra	Rb	0000000000	$Addr := Ra + Rb$ $Rd[0:23] := 0$ $Rd[24:31] := *Addr[0:7]$
LHU Rd,Ra,Rb	110001	Rd	Ra	Rb	0000000000	$Addr := Ra + Rb$ $Rd[0:15] := 0$ $Rd[16:31] := *Addr[0:15]$
LW Rd,Ra,Rb	110010	Rd	Ra	Rb	0000000000	$Addr := Ra + Rb$ $Rd := *Addr$
SB Rd,Ra,Rb	110100	Rd	Ra	Rb	0000000000	$Addr := Ra + Rb$ $*Addr[0:8] := Rd[24:31]$
SH Rd,Ra,Rb	110101	Rd	Ra	Rb	0000000000	$Addr := Ra + Rb$ $*Addr[0:16] := Rd[16:31]$
SW Rd,Ra,Rb	110110	Rd	Ra	Rb	0000000000	$Addr := Ra + Rb$ $*Addr := Rd$
LBUI Rd,Ra,Imm	111000	Rd	Ra	Imm		$Addr := Ra + s(Imm)$ $Rd[0:23] := 0$ $Rd[24:31] := *Addr[0:7]$
LHUI Rd,Ra,Imm	111001	Rd	Ra	Imm		$Addr := Ra + s(Imm)$ $Rd[0:15] := 0$ $Rd[16:31] := *Addr[0:15]$
LWI Rd,Ra,Imm	111010	Rd	Ra	Imm		$Addr := Ra + s(Imm)$ $Rd := *Addr$
SBI Rd,Ra,Imm	111100	Rd	Ra	Imm		$Addr := Ra + s(Imm)$ $*Addr[0:7] := Rd[24:31]$
SHI Rd,Ra,Imm	111101	Rd	Ra	Imm		$Addr := Ra + s(Imm)$ $*Addr[0:15] := Rd[16:31]$
SWI Rd,Ra,Imm	111110	Rd	Ra	Imm		$Addr := Ra + s(Imm)$ $*Addr := Rd$

1. Due to the many different corner cases involved in floating point arithmetic, only the normal behavior is described. A full description of the behavior can be found in Chapter 4, “MicroBlaze Instruction Set Architecture.”

Registers

MicroBlaze has an orthogonal instruction set architecture. It has thirty-two 32-bit general purpose registers and up to eighteen 32-bit special purpose registers, depending on configured options.

General Purpose Registers

The thirty-two 32-bit General Purpose Registers are numbered R0 through R31. The register file is reset on bit stream download (reset value is 0x00000000). [Figure 1-2](#) is a representation of a General Purpose Register and [Table 1-7](#) provides a description of each register and the register reset value (if existing).

Note: The register file is **not** reset by the external reset inputs: `Reset` and `Debug_Rst`.

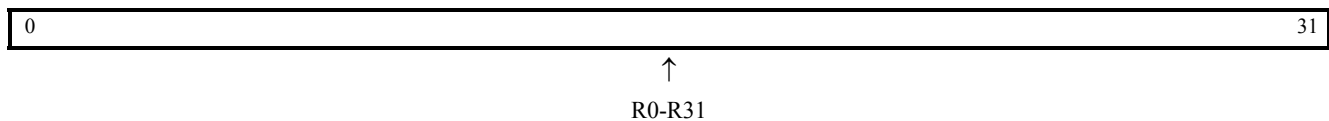


Figure 1-2: R0-R31

Table 1-7: General Purpose Registers (R0-R31)

Bits	Name	Description	Reset Value
0:31	R0	Always has a value of zero. Anything written to R0 is discarded	0x00000000
0:31	R1 through R13	32-bit general purpose registers	-
0:31	R14	32-bit register used to store return addresses for interrupts.	-
0:31	R15	32-bit general purpose register. Recommended for storing return addresses for user vectors.	-
0:31	R16	32-bit register used to store return addresses for breaks.	-
0:31	R17	If MicroBlaze is configured to support hardware exceptions, this register is loaded with the address of the instruction following the instruction causing the HW exception, except for exceptions in delay slots that use BTR instead (see “ Branch Target Register (BTR) ”); if not, it is a general purpose register.	-
0:31	R18 through R31	R18 through R31 are 32-bit general purpose registers.	-

Refer to [Table 3-2](#) for software conventions on general purpose register usage.

Special Purpose Registers

Program Counter (PC)

The Program Counter (PC) is the 32-bit address of the execution instruction. It can be read with an MFS instruction, but it cannot be written with an MTS instruction. When used with the MFS instruction the PC register is specified by setting Sa = 0x0000. Figure 1-3 illustrates the PC and Table 1-8 provides a description and reset value.

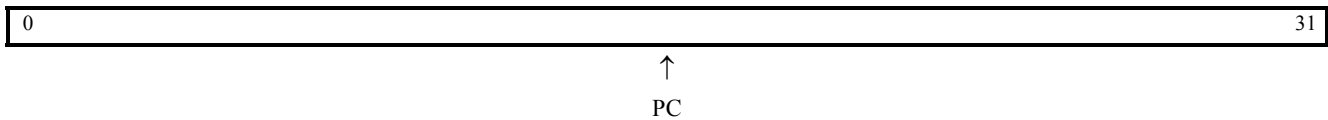


Figure 1-3: PC

Table 1-8: Program Counter (PC)

Bits	Name	Description	Reset Value
0:31	PC	Program Counter Address of executing instruction, for example, “mfs r2 0” stores the address of the mfs instruction itself in R2.	0x00000000

Machine Status Register (MSR)

The Machine Status Register contains control and status bits for the processor. It can be read with an MFS instruction. When reading the MSR, bit 29 is replicated in bit 0 as the carry copy. MSR can be written using either an MTS instruction or the dedicated MSRSET and MSRCLR instructions.

When writing to the MSR, the Carry bit takes effect immediately and the remaining bits take effect one clock cycle later. Any value written to bit 0 is discarded. When used with an MTS or MFS instruction, the MSR is specified by setting Sx = 0x0001. Figure 1-4 illustrates the MSR register and Table 1-9 provides the bit description and reset values.

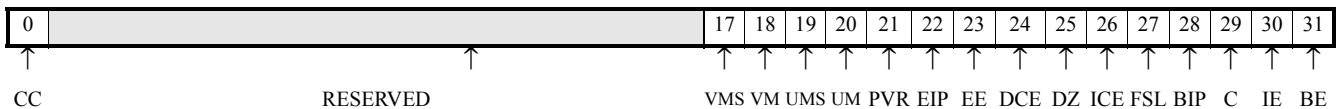


Figure 1-4: MSR

Table 1-9: Machine Status Register (MSR)

Bits	Name	Description	Reset Value
0	CC	Arithmetic Carry Copy Copy of the Arithmetic Carry (bit 29). CC is always the same as bit C.	0
1:16	Reserved		
17	VMS	Virtual Protected Mode Save Only available when configured with an MMU (if C_USE_MMU>1) Read/Write	0
18	VM	Virtual Protected Mode 0 MMU address translation and access protection disabled, with C_USE_MMU = 3. Access protection disabled, with C_USE_MMU = 2. 1 MMU address translation and access protection enabled, with C_USE_MMU = 3. Access protection enabled, with C_USE_MMU = 2. Only available when configured with an MMU (if C_USE_MMU>1) Read/Write	0
19	UMS	User Mode Save Only available when configured with an MMU (if C_USE_MMU>0) Read/Write	0
20	UM	User Mode 0 Privileged Mode, all instructions are allowed 1 User Mode, certain instructions are not allowed Only available when configured with an MMU (if C_USE_MMU>0) Read/Write	0
21	PVR	Processor Version Register exists 0 No Processor Version Register 1 Processor Version Register exists Read only	Based on parameter C_PVR

Table 1-9: Machine Status Register (MSR) (Continued)

Bits	Name	Description	Reset Value
22	EIP	Exception In Progress 0 = No hardware exception in progress 1 = Hardware exception in progress Only available if configured with exception support (C_*_EXCEPTION or C_USE_MMU) Read/Write	0
23	EE	Exception Enable 0 = Hardware exceptions disabled ¹ 1 = Hardware exceptions enabled Only available if configured with exception support (C_*_EXCEPTION or C_USE_MMU) Read/Write	0
24	DCE	Data Cache Enable 0 = Data Cache disabled 1 = Data Cache enabled Only available if configured to use data cache (C_USE_DCACHE = 1) Read/Write	0
25	DZ	Division by Zero ² 0 = No division by zero has occurred 1 = Division by zero has occurred Only available if configured to use hardware divider (C_USE_DIV = 1) Read/Write	0
26	ICE	Instruction Cache Enable 0 = Instruction Cache disabled 1 = Instruction Cache enabled Only available if configured to use instruction cache (C_USE_ICACHE = 1) Read/Write	0
27	FSL	FSL Error 0 = FSL get/getd/put/putd had no error 1 = FSL get/getd/put/putd control type mismatch Only available if configured to use FSL links (C_FSL_LINKS > 0) Read/Write	0

Table 1-9: Machine Status Register (MSR) (Continued)

Bits	Name	Description	Reset Value
28	BIP	Break in Progress 0 = No Break in Progress 1 = Break in Progress Break Sources can be software break instruction or hardware break from Ext_Brk or Ext_NM_Brk pin. Read/Write	0
29	C	Arithmetic Carry 0 = No Carry (Borrow) 1 = Carry (No Borrow) Read/Write	0
30	IE	Interrupt Enable 0 = Interrupts disabled 1 = Interrupts enabled Read/Write	0
31	BE	Buslock Enable ³ 0 = Buslock disabled on data-side PLB or OPB 1 = Buslock enabled on data-side PLB or OPB Buslock Enable does not affect operation of IXCL, DXCL, ILMB, DLMB, IPLB or IOPB. Only available if using data-side PLB or OPB Read/Write	0

1. The MMU exceptions (Data Storage Exception, Instruction Storage Exception, Data TLB Miss Exception, Instruction TLB Miss Exception) cannot be disabled, and are not affected by this bit.
2. This bit is only used for integer divide-by-zero signaling. There is a floating point equivalent in the FSR. The DZ-bit flags divide by zero conditions regardless if the processor is configured with exception handling or not.
3. For details on the bus protocols, refer to the IBM CoreConnect specifications: *128-Bit Processor Local Bus, Architectural Specifications, Version 4.6* and *64-Bit On-Chip Peripheral Bus, Architectural Specifications, Version 2.0*.

Exception Address Register (EAR)

The Exception Address Register stores the full load/store address that caused the exception for the following:

- An unaligned access exception that means the unaligned access address
- A DPLB or DOPB exception that specifies the failing PLB or OPB data access address
- A data storage exception that specifies the (virtual) effective address accessed
- An instruction storage exception that specifies the (virtual) effective address read
- A data TLB miss exception that specifies the (virtual) effective address accessed
- An instruction TLB miss exception that specifies the (virtual) effective address read

The contents of this register is undefined for all other exceptions. When read with the MFS instruction, the EAR is specified by setting Sa = 0x0003. The EAR register is illustrated in Figure 1-5 and Table 1-10 provides bit descriptions and reset values.

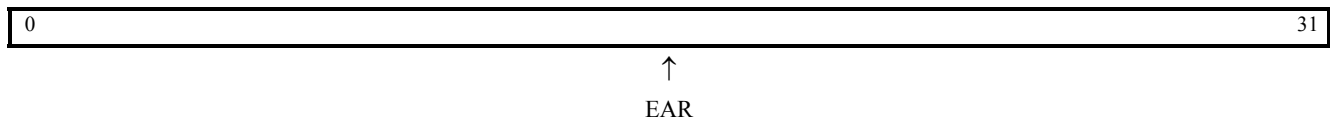


Figure 1-5: EAR

Table 1-10: Exception Address Register (EAR)

Bits	Name	Description	Reset Value
0:31	EAR	Exception Address Register	0x00000000

Exception Status Register (ESR)

The Exception Status Register contains status bits for the processor. When read with the MFS instruction, the ESR is specified by setting Sa = 0x0005. The ESR register is illustrated in [Figure 1-6](#), [Table 1-11](#) provides bit descriptions and reset values, and [Table 1-12](#) provides the Exception Specific Status (ESS).

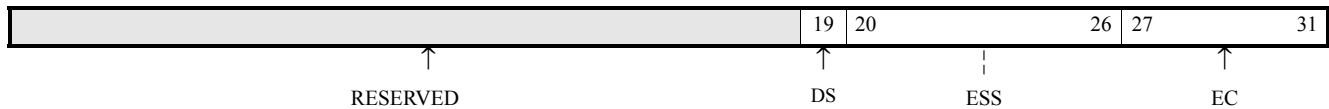


Figure 1-6: ESR

Table 1-11: Exception Status Register (ESR)

Bits	Name	Description	Reset Value
0:18	Reserved		
19	DS	Delay Slot Exception. 0 = not caused by delay slot instruction 1 = caused by delay slot instruction Read-only	0
20:26	ESS	Exception Specific Status For details refer to Table 1-12 . Read-only	See Table 1-12
27:31	EC	Exception Cause 00000 = Fast Simplex Link exception 00001 = Unaligned data access exception 00010 = Illegal op-code exception 00011 = Instruction bus error exception 00100 = Data bus error exception 00101 = Divide by zero exception 00110 = Floating point unit exception 00111 = Privileged instruction exception 10000 = Data storage exception 10001 = Instruction storage exception 10010 = Data TLB miss exception 10011 = Instruction TLB miss exception Read-only	0

Table 1-12: Exception Specific Status (ESS)

Exception Cause	Bits	Name	Description	Reset Value
Unaligned Data Access	20	W	Word Access Exception 0 = unaligned halfword access 1 = unaligned word access	0
	21	S	Store Access Exception 0 = unaligned load access 1 = unaligned store access	0
	22:26	Rx	Source/Destination Register General purpose register used as source (Store) or destination (Load) in unaligned access	0
Illegal Instruction	20:26	Reserved		0
Instruction bus error	20:26	Reserved		0
Data bus error	20:26	Reserved		0
Divide by zero	20:26	Reserved		0
Floating point unit	20:26	Reserved		0
Privileged instruction	20:26	Reserved		0
Fast Simplex Link	20:22	Reserved		0
	23:26	FSL	Fast Simplex Link index that caused the exception	0
Data storage	20	DIZ	Data storage - Zone protection 0 = Did not occur 1 = Occurred	0
	21	S	Data storage - Store instruction 0 = Did not occur 1 = Occurred	0
	22:26	Reserved		0
Instruction storage	20	DIZ	Instruction storage - Zone protection 0 = Did not occur 1 = Occurred	0
	21:26	Reserved		0

Table 1-12: Exception Specific Status (ESS) (Continued)

Exception Cause	Bits	Name	Description	Reset Value
Data TLB miss	20	Reserved		0
	21	S	Data TLB miss - Store instruction 0 = Did not occur 1 = Occurred	0
	22:26	Reserved		0
Instruction TLB miss	20:26	Reserved		0

Branch Target Register (BTR)

The Branch Target Register only exists if the MicroBlaze processor is configured to use exceptions. The register stores the branch target address for all delay slot branch instructions executed while MSR[EIP] = 0. If an exception is caused by an instruction in a delay slot (for example, ESR[DS]=1), the exception handler should return execution to the address stored in BTR instead of the normal exception return address stored in R17. When read with the MFS instruction, the BTR is specified by setting Sa = 0x000B. The BTR register is illustrated in [Figure 1-7](#) and [Table 1-13](#) provides bit descriptions and reset values.

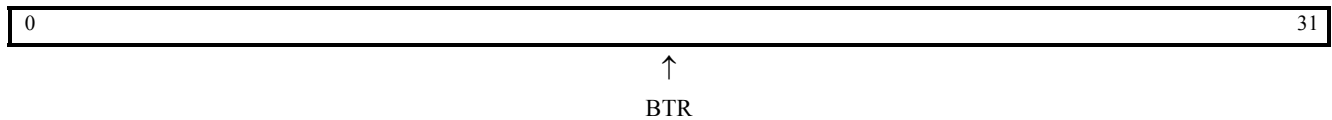


Figure 1-7: BTR

Table 1-13: Branch Target Register (BTR)

Bits	Name	Description	Reset Value
0:31	BTR	Branch target address used by handler when returning from an exception caused by an instruction in a delay slot. Read-only	0x00000000

Floating Point Status Register (FSR)

The Floating Point Status Register contains status bits for the floating point unit. It can be read with an MFS, and written with an MTS instruction. When read or written, the register is specified by setting Sa = 0x0007. Figure 1-8 illustrates the FSR register and Table 1-14 provides bit descriptions and reset values.

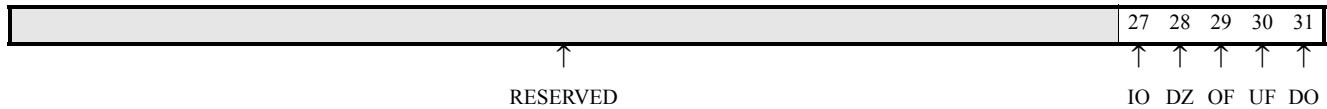


Figure 1-8: FSR

Table 1-14: Floating Point Status Register (FSR)

Bits	Name	Description	Reset Value
0:26	Reserved		undefined
27	IO	Invalid operation	0
28	DZ	Divide-by-zero	0
29	OF	Overflow	0
30	UF	Underflow	0
31	DO	Denormalized operand error	0

Exception Data Register (EDR)

The Exception Data Register stores data read on an FSL link that caused an FSL exception.

The contents of this register is undefined for all other exceptions. When read with the MFS instruction, the EAR is specified by setting Sa = 0x000D. Figure 1-9 illustrates the EDR register and Table 1-15 provides bit descriptions and reset values.

Note: The register is only implemented if C_FSL_LINKS is greater than 0 and C_FSL_EXCEPTION is set to 1.

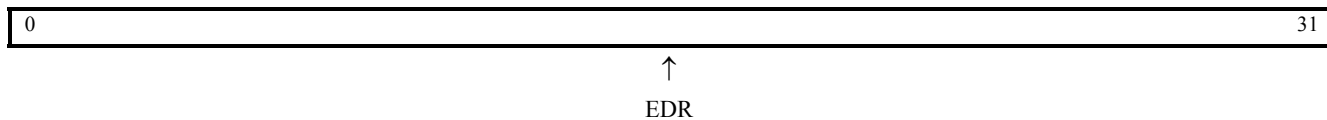


Figure 1-9: EDR

Table 1-15: Exception Address Register (EDR)

Bits	Name	Description	Reset Value
0:31	EDR	Exception Data Register	0x00000000

Process Identifier Register (PID)

The Process Identifier Register is used to uniquely identify a software process during MMU address translation. It is controlled by the C_MMU configuration option on MicroBlaze. The register is only implemented if C_MMU is greater than 1. When accessed with the MFS and MTS instructions, the PID is specified by setting Sa = 0x1000. The register is accessible according to the memory management special registers parameter C_MMU_TLB_ACCESS.

PID is also used when accessing a TLB entry:

- When writing Translation Look-Aside Buffer High (TLBHI) the value of PID is stored in the TID field of the TLB entry
- When reading TLBHI the value in the TID field is stored in PID

Figure 1-10 illustrates the PID register and Table 1-16 provides bit descriptions and reset values.

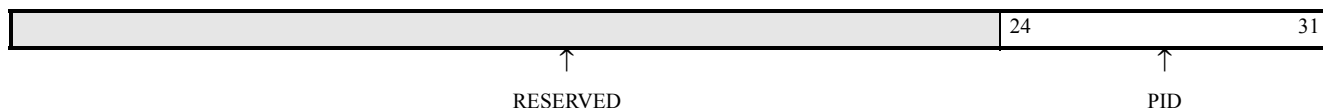


Figure 1-10: PID

Table 1-16: Process Identifier Register (PID)

Bits	Name	Description	Reset Value
0:23	Reserved		
24:31	PID	Used to uniquely identify a software process during MMU address translation. Read/Write	0x00

Zone Protection Register (ZPR)

The Zone Protection Register is used to override MMU memory protection defined in TLB entries. It is controlled by the C_MMU configuration option on MicroBlaze. The register is only implemented if C_MMU is greater than 1 and if the number of specified memory protection zones is greater than zero (C_MMU_ZONES > 0). The implemented register bits depend on the number of specified memory protection zones (C_MMU_ZONES). When accessed with the MFS and MTS instructions, the ZPR is specified by setting Sa = 0x1001. The register is accessible according to the memory management special registers parameter C_MMU_TLB_ACCESS. Figure 1-11 illustrates the ZPR register and Table 1-17 provides bit descriptions and reset values.

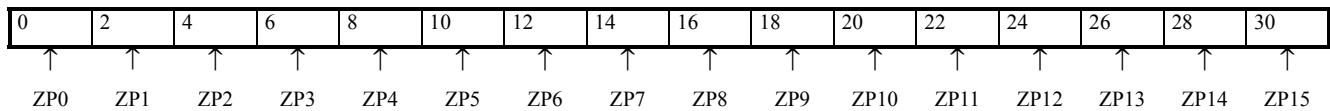


Figure 1-11: ZPR

Table 1-17: Zone Protection Register (ZPR)

Bits	Name	Description	Reset Value
0:1	ZP0	Zone Protect	0x00000000
2:3	ZP1	User mode (MSR[UM] = 1):	
...	...	00 = Override V in TLB entry. No access to the page is allowed	
30:31	ZP15	01 = No override. Use V, WR and EX from TLB entry 10 = No override. Use V, WR and EX from TLB entry 11 = Override WR and EX in TLB entry. Access the page as writable and executable	
		Privileged mode (MSR[UM] = 0): 00 = No override. Use V, WR and EX from TLB entry 01 = No override. Use V, WR and EX from TLB entry 10 = Override WR and EX in TLB entry. Access the page as writable and executable 11 = Override WR and EX in TLB entry. Access the page as writable and executable	
		Read/Write	

Translation Look-Aside Buffer Low Register (TLBLO)

The Translation Look-Aside Buffer Low Register is used to access MMU Unified Translation Look-Aside Buffer (UTLB) entries. It is controlled by the C_MMU configuration option on MicroBlaze. The register is only implemented if C_MMU is greater than 1. When accessed with the MFS and MTS instructions, the TLBLO is specified by setting Sa = 0x1002. When reading or writing TLBLO, the UTLB entry indexed by the TLBX register is accessed. The register is readable according to the memory management special registers parameter C_MMU_TLB_ACCESS.

The UTLB is reset on bit stream download (reset value is 0x00000000 for all TLBLO entries).

Note: The UTLB is **not** reset by the external reset inputs: Reset and Debug_Rst.

Figure 1-12 illustrates the TLBLO register and Table 1-18 provides bit descriptions and reset values.

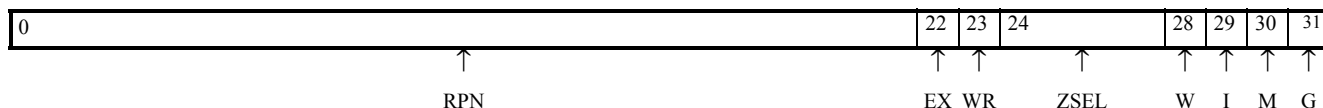


Figure 1-12: TLBLO

Table 1-18: Translation Look-Aside Buffer Low Register (TLBLO)

Bits	Name	Description	Reset Value
0:21	RPN	Real Page Number or Physical Page Number When a TLB hit occurs, this field is read from the TLB entry and is used to form the physical address. Depending on the value of the SIZE field, some of the RPN bits are not used in the physical address. Software must clear unused bits in this field to zero. Only defined when C_USE_MMU=3. Read/Write	0x000000
22	EX	Executable When bit is set to 1, the page contains executable code, and instructions can be fetched from the page. When bit is cleared to 0, instructions cannot be fetched from the page. Attempts to fetch instructions from a page with a clear EX bit cause an instruction-storage exception. Read/Write	0

Table 1-18: Translation Look-Aside Buffer Low Register (TLBLO) (Continued)

Bits	Name	Description	Reset Value
23	WR	Writable When bit is set to 1, the page is writable and store instructions can be used to store data at addresses within the page. When bit is cleared to 0, the page is read-only (not writable). Attempts to store data into a page with a clear WR bit cause a data storage exception. Read/Write	0
24:27	ZSEL	Zone Select This field selects one of 16 zone fields (Z0-Z15) from the zone-protection register (ZPR). For example, if ZSEL 0x5, zone field Z5 is selected. The selected ZPR field is used to modify the access protection specified by the TLB entry EX and WR fields. It is also used to prevent access to a page by overriding the TLB V (valid) field. Read/Write	0x0
28	W	Write Through This bit is fixed to 1, because accesses to pages on MicroBlaze are always cached using a write-through caching policy. Read Only	1
29	I	Inhibit Caching When bit is set to 1, accesses to the page are not cached (caching is inhibited). When cleared to 0, accesses to the page are cacheable. Read/Write	0
30	M	Memory Coherent This bit is fixed to 0, because memory coherence is not implemented on MicroBlaze. Read Only	0
31	G	Guarded When bit is set to 1, speculative page accesses are not allowed (memory is guarded). When cleared to 0, speculative page accesses are allowed. The G attribute can be used to protect memory-mapped I/O devices from inappropriate instruction accesses. Read/Write	0

Translation Look-Aside Buffer High Register (TLBHI)

The Translation Look-Aside Buffer High Register is used to access MMU Unified Translation Look-Aside Buffer (UTLB) entries. It is controlled by the C_MMU configuration option on MicroBlaze. The register is only implemented if C_MMU is greater than 1. When accessed with the MFS and MTS instructions, the TLBHI is specified by setting Sa = 0x1003. When reading or writing TLBHI, the UTLB entry indexed by the TLBX register is accessed. The register is readable according to the memory management special registers parameter C_MMU_TLB_ACCESS.

PID is also used when accessing a TLB entry:

- When writing TLBHI the value of PID is stored in the TID field of the TLB entry
- When reading TLBHI the value in the TID field is stored in PID

The UTLB is reset on bit stream download (reset value is 0x00000000 for all TLBHI entries).

Note: The UTLB is **not** reset by the external reset inputs: Reset and Debug_Rst.

Figure 1-13 illustrates the TLBHI register and Table 1-19 provides bit descriptions and reset values.

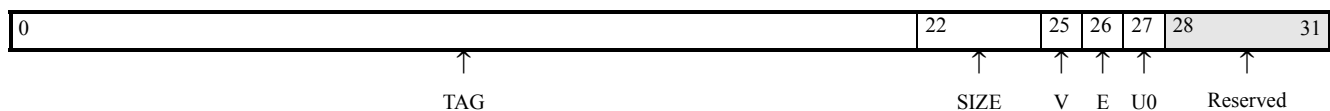


Figure 1-13: TLBHI

Table 1-19: Translation Look-Aside Buffer High Register (TLBHI)

Bits	Name	Description	Reset Value
0:21	TAG	TLB-entry tag Is compared with the page number portion of the virtual memory address under the control of the SIZE field. Read/Write	0x000000
22:24	SIZE	Size Specifies the page size. The SIZE field controls the bit range used in comparing the TAG field with the page number portion of the virtual memory address. Read/Write	000
25	V	Valid When bit is set to 1, the TLB entry is valid and contains a page-translation entry. When cleared to 0, the TLB entry is invalid. Read/Write	0

Table 1-19: Translation Look-Aside Buffer High Register (TLBHI) (Continued)

Bits	Name	Description	Reset Value
26	E	Endian This bit is fixed to 0, since accesses to pages on MicroBlaze are always big endian. Read Only	0
27	U0	User Defined This bit is fixed to 0, since there are no user defined storage attributes on MicroBlaze. Read Only	0
28:31	Reserved		

Translation Look-Aside Buffer Index Register (TLBX)

The Translation Look-Aside Buffer Index Register is used as an index to the Unified Translation Look-Aside Buffer (UTLB) when accessing the TLBLO and TLBHI registers. It is controlled by the C_MMU configuration option on MicroBlaze. The register is only implemented if C_MMU is greater than 1. When accessed with the MFS and MTS instructions, the TLBX is specified by setting Sa = 0x1004. [Figure 1-14](#) illustrates the TLBX register and [Table 1-20](#) provides bit descriptions and reset values.

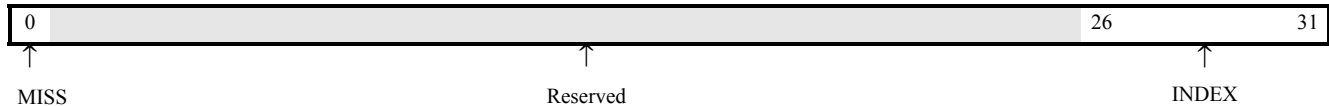


Figure 1-14: TLBX

Table 1-20: Translation Look-Aside Buffer Index Register (TLBX)

Bits	Name	Description	Reset Value
0	MISS	<p>TLB Miss</p> <p>This bit is cleared to 0 when the TLBSX register is written with a virtual address, and the virtual address is found in a TLB entry.</p> <p>The bit is set to 1 if the virtual address is not found. It is also cleared when the TLBX register itself is written.</p> <p>Read Only</p> <p>Can be read if the memory management special registers parameter C_MMU_TLB_ACCESS > 0.</p>	0
1:25	Reserved		
26:31	INDEX	<p>TLB Index</p> <p>This field is used to index the Translation Look-Aside Buffer entry accessed by the TLBLO and TLBHI registers. The field is updated with a TLB index when the TLBSX register is written with a virtual address, and the virtual address is found in the corresponding TLB entry.</p> <p>Read/Write</p> <p>Can be read and written if the memory management special registers parameter C_MMU_TLB_ACCESS > 0.</p>	000000

Translation Look-Aside Buffer Search Index Register (TLBSX)

The Translation Look-Aside Buffer Search Index Register is used to search for a virtual page number in the Unified Translation Look-Aside Buffer (UTLB). It is controlled by the C_MMU configuration option on MicroBlaze. The register is only implemented if C_MMU is greater than 1. When written with the MTS instruction, the TLBSX is specified by setting Sa = 0x1005. Figure 1-15 illustrates the TLBSX register and Table 1-21 provides bit descriptions and reset values.

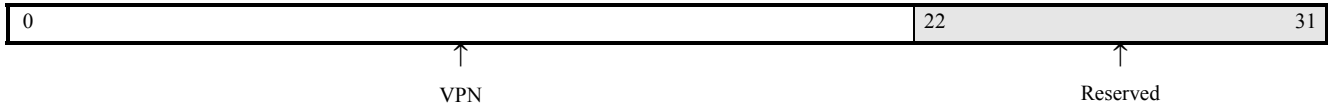


Figure 1-15: TLBSX

Table 1-21: Translation Look-Aside Buffer Index Search Register (TLBSX)

Bits	Name	Description	Reset Value
0:21	VPN	<p>Virtual Page Number</p> <p>This field represents the page number portion of the virtual memory address. It is compared with the page number portion of the virtual memory address under the control of the SIZE field, in each of the Translation Look-Aside Buffer entries that have the V bit set to 1.</p> <p>If the virtual page number is found, the TLBX register is written with the index of the TLB entry and the MISS bit in TLBX is cleared to 0. If the virtual page number is not found in any of the TLB entries, the MISS bit in the TLBX register is set to 1.</p> <p>Write Only</p>	
22:31	Reserved		

Processor Version Register (PVR)

The Processor Version Register is controlled by the C_PVR configuration option on MicroBlaze.

- When C_PVR is set to 0 the processor does not implement any PVR and MSR[PVR]=0.
- When C_PVR is set to 1, MicroBlaze implements only the first register: PVR0, and if set to 2, all 12 PVR registers (PVR0 to PVR11) are implemented.

When read with the MFS instruction the PVR is specified by setting Sa = 0x200x, with x being the register number between 0x0 and 0xB.

Table 1-22 through Table 1-32 provide bit descriptions and values.

Table 1-22: Processor Version Register 0 (PVR0)

Bits	Name	Description	Value
0	CFG	PVR implementation: 0=basic, 1=full	Based on C_PVR
1	BS	Use barrel shifter	C_USE_BARREL
2	DIV	Use divider	C_USE_DIV
3	MUL	Use hardware multiplier	C_USE_HW_MUL > 0
4	FPU	Use FPU	C_USE_FPU > 0
5	EXC	Use any type of exceptions	Based on C_*_EXCEPTION
6	ICU	Use instruction cache	C_USE_ICACHE
7	DCU	Use data cache	C_USE_DCACHE
8	MMU	Use MMU	C_USE_MMU > 0
9:15	Reserved		0
16:23	MBV	MicroBlaze release version code 0x1 = v5.00.a 0x2 = v5.00.b 0x3 = v5.00.c 0x4 = v6.00.a 0x6 = v6.00.b 0x5 = v7.00.a	Release Specific
24:31	USR1	User configured value 1	C_PVR_USER1

Table 1-23: Processor Version Register 1 (PVR1)

Bits	Name	Description	Value
0:31	USR2	User configured value 2	C_PVR_USER2

Table 1-24: Processor Version Register 2 (PVR2)

Bits	Name	Description	Value
0	DOPB	Data side OPB in use	C_D_OPB
1	DLMB	Data side LMB in use	C_D_LMB
2	IOPB	Instruction side OPB in use	C_I_OPB
3	ILMB	Instruction side LMB in use	C_I_LMB
4	IRQEDGE	Interrupt is edge triggered	C_INTERRUPT_IS_EDGE
5	IRQPOS	Interrupt edge is positive	C_EDGE_IS_POSITIVE
6	DPLB	Data side PLB in use	C_D_PLB
7	IPLB	Instruction side PLB in use	C_I_PLB
8	INTERCON	Use PLB interconnect	C_INTERCONNECT
9:11	Reserved		
12	FSL	Use extended FSL instructions	C_USE_EXTENDED_FSL_INSTR
13	FSLEXC	Generate exception for FSL control bit mismatch	C_FSL_EXCEPTION
14	MSR	Use mrsset and msrclr instructions	C_USE_MSR_INSTR
15	PCMP	Use pattern compare instructions	C_USE_PCMP_INSTR
16	AREA	Optimize area	C_AREA_OPTIMIZED
17	BS	Use barrel shifter	C_USE_BARREL
18	DIV	Use divider	C_USE_DIV
19	MUL	Use hardware multiplier	C_USE_HW_MUL > 0
20	FPU	Use FPU	C_USE_FPU > 0
21	MUL64	Use 64-bit hardware multiplier	C_USE_HW_MUL = 2
22	FPU2	Use floating point conversion and square root instructions	C_USE_FPU = 2
23	IPLBEXC	Generate exception for IPLB error	C_IPLB_BUS_EXCEPTION
24	DPLBEXC	Generate exception for DPLB error	C_DPLB_BUS_EXCEPTION
25	OP0EXC	Generate exception for 0x0 illegal opcode	C_OPCODE_0x0_ILLEGAL
26	UNEXC	Generate exception for unaligned data access	C_UNALIGNED_EXCEPTION

Table 1-24: Processor Version Register 2 (PVR2) (Continued)

Bits	Name	Description	Value
27	OPEXC	Generate exception for any illegal opcode	C_ILL_OPCODE_EXCEPTION
28	IOPBEXC	Generate exception for IOPB error	C_IOPB_BUS_EXCEPTION
29	DOPBEXC	Generate exception for DOPB error	C_DOPB_BUS_EXCEPTION
30	DIVEXC	Generate exception for division by zero	C_DIV_ZERO_EXCEPTION
31	FPUEXC	Generate exceptions from FPU	C_FPU_EXCEPTION

Table 1-25: Processor Version Register 4 (PVR4)

Bits	Name	Description	Value
0	ICU	Use instruction cache	C_USE_ICACHE
1:5	ICTS	Instruction cache tag size	C_ADDR_TAG_BITS
6	Reserved		1
7	ICW	Allow instruction cache write	C_ALLOW_ICACHE_WR
8:10	ICLL	The base two logarithm of the instruction cache line length	$\log_2(C_ICACHE_LINE_LEN)$
11:15	ICBS	The base two logarithm of the instruction cache byte size	$\log_2(C_DCACHE_BYTE_SIZE)$
16:31	Reserved		0

Table 1-26: Processor Version Register 5 (PVR5)

Bits	Name	Description	Value
0	DCU	Use data cache	C_USE_DCACHE
1:5	DCTS	Data cache tag size	C_DCACHE_ADDR_TAG
6	Reserved		1
7	DCW	Allow data cache write	C_ALLOW_DCACHE_WR
8:10	DCLL	The base two logarithm of the data cache line length	$\log_2(C_DCACHE_LINE_LEN)$
11:15	DCBS	The base two logarithm of the data cache byte size	$\log_2(C_DCACHE_BYTE_SIZE)$
16:31	Reserved		0

Table 1-27: Processor Version Register 6 (PVR6)

Bits	Name	Description	Value
0:31	ICBA	Instruction Cache Base Address	C_ICACHE_BASEADDR

Table 1-28: Processor Version Register 7 (PVR7)

Bits	Name	Description	Value
0:31	ICHA	Instruction Cache High Address	C_ICACHE_HIGHADDR

Table 1-29: Processor Version Register 8 (PVR8)

Bits	Name	Description	Value
0:31	DCBA	Data Cache Base Address	C_DCACHE_BASEADDR

Table 1-30: Processor Version Register 9 (PVR9)

Bits	Name	Description	Value
0:31	DCHA	Data Cache High Address	C_DCACHE_HIGHADDR

Table 1-31: Processor Version Register 10 (PVR10)

Bits	Name	Description	Value
0:7	ARCH	Target architecture: 0x4 = Virtex™2 0x5 = Virtex2Pro 0x6 = Spartan™3 0x7 = Virtex4 0x8 = Virtex5 0x9 = Spartan3E 0xA = Spartan3A 0xB = Spartan3AN 0xC = Spartan3Adsp	Defined by parameter C_FAMILY
8:31	Reserved		0

Table 1-32: Processor Version Register 11 (PVR11)

Bits	Name	Description	Value
0:1	MMU	Use MMU: 0 = None 1 = User Mode 2 = Protection 3 = Virtual	C_USE:_MMU
2:4	ITLB	Instruction Shadow TLB size	$\log_2(C_MMU_ITLB_SIZE)$
5:7	DTLB	Data Shadow TLB size	$\log_2(C_MMU_DTLB_SIZE)$
8:9	TLBACC	TLB register access: 0 = Minimal 1 = Read 2 = Write 3 = Full	C_MMU_TLB_ACCESS
10:14	ZONES	Number of memory protection zones	C_MMU_ZONES
15:20	Reserved	Reserved for future use	0
21:31	RSTMSR	Reset value for MSR	C_RESET_MSR

Pipeline Architecture

MicroBlaze instruction execution is pipelined. For most instructions, each stage takes one clock cycle to complete. Consequently, the number of clock cycles necessary for a specific instruction to complete is equal to the number of pipeline stages, and one instruction is completed on every cycle. A few instructions require multiple clock cycles in the execute stage to complete. This is achieved by stalling the pipeline.

When executing from slower memory, instruction fetches may take multiple cycles. This additional latency directly affects the efficiency of the pipeline. MicroBlaze implements an instruction prefetch buffer that reduces the impact of such multi-cycle instruction memory latency. While the pipeline is stalled by a multi-cycle instruction in the execution stage, the prefetch buffer continues to load sequential instructions. When the pipeline resumes execution, the fetch stage can load new instructions directly from the prefetch buffer instead of waiting for the instruction memory access to complete.

Three Stage Pipeline

When area optimization is enabled, the pipeline is divided into three stages to minimize hardware cost: Fetch, Decode, and Execute.

	cycle 1	cycle 2	cycle 3	cycle4	cycle5	cycle6	cycle7
instruction 1	Fetch	Decode	Execute				
instruction 2		Fetch	Decode	Execute	Execute	Execute	
instruction 3			Fetch	Decode	Stall	Stall	Execute

Five Stage Pipeline

When area optimization is disabled, the pipeline is divided into five stages to maximize performance: Fetch (IF), Decode (OF), Execute (EX), Access Memory (MEM), and Writeback (WB).

	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle 9
instruction 1	IF	OF	EX	MEM	WB				
instruction 2		IF	OF	EX	MEM	MEM	MEM	WB	
instruction 3			IF	OF	EX	Stall	Stall	MEM	WB

Branches

Normally the instructions in the fetch and decode stages (as well as prefetch buffer) are flushed when executing a taken branch. The fetch pipeline stage is then reloaded with a new instruction from the calculated branch address. A taken branch in MicroBlaze takes three clock cycles to execute, two of which are required for refilling the pipeline. To reduce this latency overhead, MicroBlaze supports branches with delay slots.

Delay Slots

When executing a taken branch with delay slot, only the fetch pipeline stage in MicroBlaze is flushed. The instruction in the decode stage (branch delay slot) is allowed to complete. This technique effectively reduces the branch penalty from two clock cycles to one. Branch instructions with delay slots have a D appended to the instruction mnemonic. For example, the BNE instruction does not execute the subsequent instruction (does not have a delay slot), whereas BNED executes the next instruction before control is transferred to the branch location.

A delay slot must not contain the following instructions: IMM, branch, or break. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

Instructions that could cause recoverable exceptions (e.g. unaligned word or halfword load and store) are allowed in the delay slot. If an exception is caused in a delay slot the ESR[DS] bit is set, and the exception handler is responsible for returning the execution to the branch target (stored in the special purpose register BTR). If the ESR[DS] bit is set, register R17 is not valid (otherwise it contains the address following the instruction causing the exception).

Memory Architecture

MicroBlaze is implemented with a Harvard memory architecture; instruction and data accesses are done in separate address spaces. Each address space has a 32-bit range (for example, handles up to 4-Gb of instructions and data memory respectively). The instruction and data memory ranges can be made to overlap by mapping them both to the same physical memory. The latter is useful for software debugging.

Both instruction and data interfaces of MicroBlaze are 32 bits wide and use big endian, bit-reversed format. MicroBlaze supports word, halfword, and byte accesses to data memory.

Data accesses must be aligned (word accesses must be on word boundaries, halfword on halfword boundaries), unless the processor is configured to support unaligned exceptions. All instruction accesses must be word aligned.

MicroBlaze does not separate data accesses to I/O and memory (it uses memory mapped I/O). The processor has up to three interfaces for memory accesses:

- Local Memory Bus (LMB)
- Processor Local Bus (PLB) or On-Chip Peripheral Bus (OPB)
- Xilinx CacheLink (XCL)

The LMB memory address range must not overlap with PLB, OPB or XCL ranges.

MicroBlaze has a single cycle latency for accesses to local memory (LMB) and for cache read hits, except with area optimization enabled when data side accesses and data cache read hits require two clock cycles. A data cache write normally has two cycles of latency (more if the posted-write buffer in the memory controller is full).

The MicroBlaze instruction and data caches can be configured to use 4 or 8 word cache lines. When using a longer cache line, more bytes are prefetched, which generally improves performance for software with sequential access patterns. However, for software with a more random access pattern the performance can instead decrease for a given cache size. This is caused by a reduced cache hit rate due to fewer available cache lines.

For details on the different memory interfaces refer to [Chapter 2, “MicroBlaze Signal Interface Description”](#).

Privileged Instructions

The following MicroBlaze instructions are privileged:

- GET, PUT, NGET, NPUT, CGET, CPUT, NCGET, NCPUT
- WIC, WDC
- MTS
- MSRCLR, MSRSET (except when only the C bit is affected)
- BRK
- RTID, RTBD, RTED
- BRKI (except when jumping to physical address 0x8 or 0x18)

Attempted use of these instructions when running in user mode causes a privileged instruction exception.

There are six ways to leave user mode and virtual mode:

1. Hardware generated reset (including debug reset)
2. Hardware exception
3. Non-maskable break or hardware break
4. Interrupt
5. Executing the instruction "BRALID Re, 0x8" to perform a user vector exception
6. Executing the software break instructions "BRKI" jumping to physical address 0x8 or 0x18

In all of these cases, except hardware generated reset, the user mode and virtual mode status is saved in the MSR UMS and VMS bits.

Application (user-mode) programs transfer control to system-service routines (privileged mode programs) using the BRALID or BRKI instruction, jumping to physical address 0x8. Executing this instruction causes a system-call exception to occur. The exception handler determines which system-service routine to call and whether the calling application has permission to call that service. If permission is granted, the exception handler performs the actual procedure call to the system-service routine on behalf of the application program.

The execution environment expected by the system-service routine requires the execution of prologue instructions to set up that environment. Those instructions usually create the block of storage that holds procedural information (the activation record), update and initialize pointers, and save volatile registers (registers the system-service routine uses). Prologue code can be inserted by the linker when creating an executable module, or it can be included as stub code in either the system-call interrupt handler or the system-library routines.

Returns from the system-service routine reverse the process described above. Epilog code is executed to unwind and deallocate the activation record, restore pointers, and restore volatile registers. The interrupt handler executes a return from exception instruction (RTED) to return to the application.

Virtual-Memory Management

Programs running on MicroBlaze use effective addresses to access a flat 4 Gb address space. The processor can interpret this address space in one of two ways, depending on the translation mode:

- In real mode, effective addresses are used to directly access physical memory
- In virtual mode, effective addresses are translated into physical addresses by the virtual-memory management hardware in the processor

Virtual mode provides system software with the ability to relocate programs and data anywhere in the physical address space. System software can move inactive programs and data out of physical memory when space is required by active programs and data.

Relocation can make it appear to a program that more memory exists than is actually implemented by the system. This frees the programmer from working within the limits imposed by the amount of physical memory present in a system. Programmers do not need to know which physical-memory addresses are assigned to other software processes and hardware devices. The addresses visible to programs are translated into the appropriate physical addresses by the processor.

Virtual mode provides greater control over memory protection. Blocks of memory as small as 1 KB can be individually protected from unauthorized access. Protection and relocation enable system software to support multitasking. This capability gives the appearance of simultaneous or near-simultaneous execution of multiple programs.

In MicroBlaze, virtual mode is implemented by the memory-management unit (MMU), available when `C_USE_MMU` is set to 3. The MMU controls effective-address to physical-address mapping and supports memory protection. Using these capabilities, system software can implement demand-paged virtual memory and other memory management schemes.

The MicroBlaze MMU implementation is based upon PowerPC™ 405. For details, see the *PowerPC Processor Reference Guide* document.

The MMU features are summarized as follows:

- Translates effective addresses into physical addresses
- Controls page-level access during address translation
- Provides additional virtual-mode protection control through the use of zones
- Provides independent control over instruction-address and data-address translation and protection
- Supports eight page sizes: 1 kB, 4 kB, 16 kB, 64 kB, 256 kB, 1 MB, 4 MB, and 16 MB. Any combination of page sizes can be used by system software
- Software controls the page-replacement strategy

Real Mode

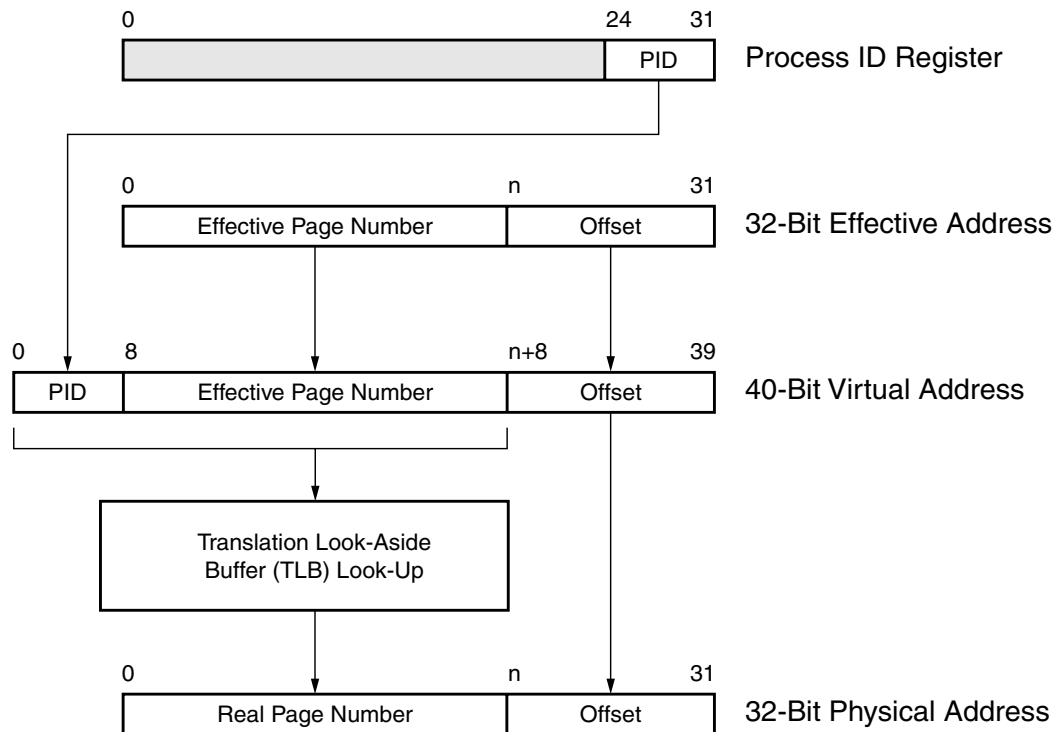
The processor references memory when it fetches an instruction and when it accesses data with a load or store instruction. Programs reference memory locations using a 32-bit effective address calculated by the processor. When real mode is enabled, the physical address is identical to the effective address and the processor uses it to access physical memory. After a processor reset, the processor operates in real mode. Real mode can also be enabled by clearing the VM bit in the MSR.

Physical-memory data accesses (loads and stores) are performed in real mode using the effective address. Real mode does not provide system software with virtual address translation, but the full memory access-protection is available, implemented when `C_USE_MMU > 1`. Implementation of a real-mode memory manager is more straightforward than a virtual-mode memory manager. Real

mode is often an appropriate solution for memory management in simple embedded environments, when access-protection is necessary, but virtual address translation is not required.

Virtual Mode

In virtual mode, the processor translates an effective address into a physical address using the process shown in Figure 1-16. Virtual mode can be enabled by setting the VM bit in the MSR.



UG011_37_021302

Figure 1-16: Virtual-Mode Address Translation

Each address shown in Figure 1-16 contains a page-number field and an offset field. The page number represents the portion of the address translated by the MMU. The offset represents the byte offset into a page and is not translated by the MMU. The virtual address consists of an additional field, called the process ID (PID), which is taken from the PID register (see Process-ID Register, page 176). The combination of PID and effective page number (EPN) is referred to as the virtual page number (VPN). The value n is determined by the page size, as shown in Table 1-33.

System software maintains a page-translation table that contains entries used to translate each virtual page into a physical page. The page size defined by a page translation entry determines the size of the page number and offset fields. For example, when a 4 kB page size is used, the page-number field is 20 bits and the offset field is 12 bits. The VPN in this case is 28 bits.

Then the most frequently used page translations are stored in the translation look-aside buffer (TLB). When translating a virtual address, the MMU examines the page-translation entries for a matching VPN (PID and EPN). Rather than examining all entries in the table, only entries contained in the processor TLB are examined. When a page-translation entry is found with a matching VPN, the corresponding physical-page number is read from the entry and combined with the offset to form the 32-bit physical address. This physical address is used by the processor to reference memory.

System software can use the PID to uniquely identify software processes (tasks, subroutines, threads) running on the processor. Independently compiled processes can operate in effective-address regions that overlap each other. This overlap must be resolved by system software if multitasking is supported. Assigning a PID to each process enables system software to resolve the overlap by relocating each process into a unique region of virtual-address space. The virtual-address space mappings enable independent translation of each process into the physical-address space.

Page-Translation Table

The page-translation table is a software-defined and software-managed data structure containing page translations. The requirement for software-managed page translation represents an architectural trade-off targeted at embedded-system applications. Embedded systems tend to have a tightly controlled operating environment and a well-defined set of application software. That environment enables virtual-memory management to be optimized for each embedded system in the following ways:

- The page-translation table can be organized to maximize page-table search performance (also called table walking) so that a given page-translation entry is located quickly. Most general-purpose processors implement either an indexed page table (simple search method, large page-table size) or a hashed page table (complex search method, small page-table size). With software table walking, any hybrid organization can be employed that suits the particular embedded system. Both the page-table size and access time can be optimized.
- Independent page sizes can be used for application modules, device drivers, system service routines, and data. Independent page-size selection enables system software to more efficiently use memory by reducing fragmentation (unused memory). For example, a large data structure can be allocated to a 16 MB page and a small I/O device-driver can be allocated to a 1 KB page.
- Page replacement can be tuned to minimize the occurrence of missing page translations. As described in the following section, the most-frequently used page translations are stored in the translation look-aside buffer (TLB). Software is responsible for deciding which translations are stored in the TLB and which translations are replaced when a new translation is required. The replacement strategy can be tuned to avoid thrashing, whereby page-translation entries are constantly being moved in and out of the TLB. The replacement strategy can also be tuned to prevent replacement of critical-page translations, a process sometimes referred to as page locking.

The unified 64-entry TLB, managed by software, caches a subset of instruction and data page-translation entries accessible by the MMU. Software uses the unified TLB to cache a subset of instruction and data page-translation entries for use by the MMU. Software is responsible for reading entries from the page-translation table in system memory and storing them in the TLB. The following section describes the unified TLB in more detail. Internally, the MMU also contains shadow TLBs for instructions and data, with sizes configurable by `C_MMU_ITLB_SIZE` and `C_MMU_DTLB_SIZE` respectively.

These shadow TLBs are managed entirely by the processor (transparent to software) and are used to minimize access conflicts with the unified TLB.

Translation Look-Aside Buffer

The translation look-aside buffer (TLB) is used by the MicroBlaze MMU for address translation when the processor is running in virtual mode, memory protection, and storage control. Each entry within the TLB contains the information necessary to identify a virtual page (PID and effective page number), specify its translation into a physical page, determine the protection characteristics of the page, and specify the storage attributes associated with the page.

The MicroBlaze TLB is physically implemented as three separate TLBs:

- Unified TLB—The UTLB contains 64 entries and is pseudo-associative. Instruction-page and data-page translation can be stored in any UTLB entry. The initialization and management of the UTLB is controlled completely by software.
- Instruction Shadow TLB—The ITLB contains instruction page-translation entries and is fully associative. The page-translation entries stored in the ITLB represent the most-recently accessed instruction-page translations from the UTLB. The ITLB is used to minimize contention between instruction translation and UTLB-update operations. The initialization and management of the ITLB is controlled completely by hardware and is transparent to software.
- Data Shadow TLB—The DTLB contains data page-translation entries and is fully associative. The page-translation entries stored in the DTLB represent the most-recently accessed data-page translations from the UTLB. The DTLB is used to minimize contention between data translation and UTLB-update operations. The initialization and management of the DTLB is controlled completely by hardware and is transparent to software.

Figure 1-17 provides the translation flow for TLB.

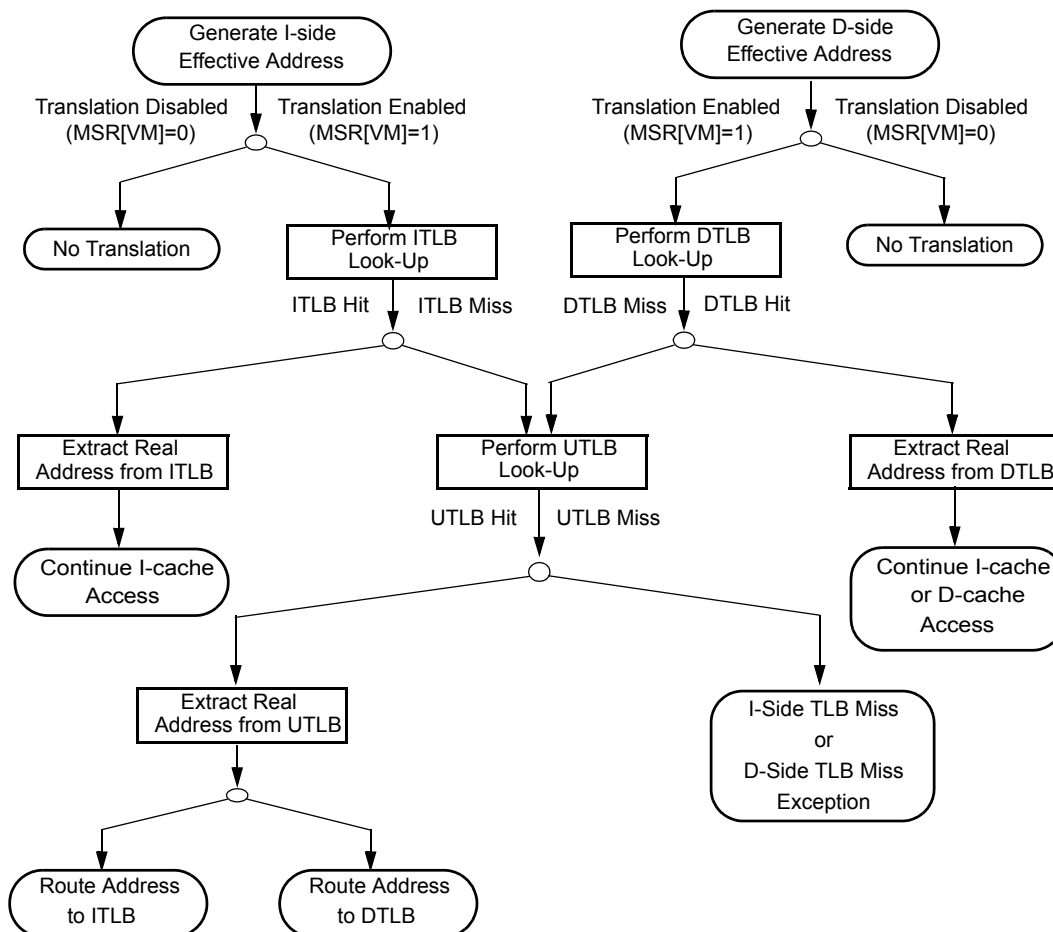


Figure 1-17: TLB Address Translation Flow

TLB Entry Format

Figure 1-18 shows the format of a TLB entry. Each TLB entry is 68 bits and is composed of two portions: TLBLO (also referred to as the data entry), and TLBHI (also referred to as the tag entry).



Figure 1-18: TLB Entry Format

The TLB entry contents are described in Table 1-18, page 33 and Table 1-19, page 35.

The fields within a TLB entry are categorized as follows:

- Virtual-page identification (TAG, SIZE, V, TID)—These fields identify the page-translation entry. They are compared with the virtual-page number during the translation process.
- Physical-page identification (RPN, SIZE)—These fields identify the translated page in physical memory.
- Access control (EX, WR, ZSEL)—These fields specify the type of access allowed in the page and are used to protect pages from improper accesses.
- Storage attributes (W, I, M, G, E, UO)—These fields specify the storage-control attributes, such as whether a page is cacheable and how bytes are ordered (endianness).

Table 1-33 shows the relationship between the TLB-entry SIZE field and the translated page size. This table also shows how the page size determines which address bits are involved in a tag comparison, which address bits are used as a page offset, and which bits in the physical page number are used in the physical address.

Table 1-33: Page-Translation Bit Ranges by Page Size

Page Size	SIZE (TLBHI Field)	Tag Comparison Bit Range	Page Offset	Physical Page Number	RPN Bits Clear to 0
1 KB	000	TAG[0:21] - Address[0:21]	Address[22:31]	RPN[0:21]	-
4 KB	001	TAG[0:19] - Address[0:19]	Address[20:31]	RPN[0:19]	20:21
16 KB	010	TAG[0:17] - Address[0:17]	Address[18:31]	RPN[0:17]	18:21
64 KB	011	TAG[0:15] - Address[0:15]	Address[16:31]	RPN[0:15]	16:21
256 KB	100	TAG[0:13] - Address[0:13]	Address[14:31]	RPN[0:13]	14:21
1 MB	101	TAG[0:11] - Address[0:11]	Address[12:31]	RPN[0:11]	12:21
4 MB	110	TAG[0:9] - Address[0:9]	Address[10:31]	RPN[0:9]	10:21
16 MB	111	TAG[0:7] - Address[0:7]	Address[8:31]	RPN[0:7]	8:21

When assigning sizes to instruction pages, software must be careful to avoid creating the opportunity for instruction-cache synonyms.

TLB Access

When the MMU translates a virtual address (the combination of PID and effective address) into a physical address, it first examines the appropriate shadow TLB for the page translation entry. If an entry is found, it is used to access physical memory. If an entry is not found, the MMU examines the UTLB for the entry. A delay occurs each time the UTLB must be accessed due to a shadow TLB miss. The miss latency ranges from 2-32 cycles. The DTLB has priority over the ITLB if both simultaneously access the UTLB.

[Figure 1-19, page 54](#) shows the logical process the MMU follows when examining a page-translation entry in one of the shadow TLBs or the UTLB. All valid entries in the TLB are checked.

A TLB hit occurs when all of the following conditions are met by a TLB entry:

- The entry is valid
- The TAG field in the entry matches the effective address EPN under the control of the SIZE field in the entry
- The TID field in the entry matches the PID

If any of the above conditions are not met, a TLB miss occurs. A TLB miss causes an exception, described as follows:

A TID value of 0x00 causes the MMU to ignore the comparison between the TID and PID. Only the TAG and EA[EPN] are compared. A TLB entry with TID=0x00 represents a process-independent translation. Pages that are accessed globally by all processes should be assigned a TID value of 0x00. A PID value of 0x00 does not identify a process that can access any page. When PID=0x00, a page-translation hit only occurs when TID=0x00. It is possible for software to load the TLB with multiple entries that match an EA[EPN] and PID combination. However, this is considered a programming error and results in undefined behavior.

When a hit occurs, the MMU reads the RPN field from the corresponding TLB entry. Some or all of the bits in this field are used, depending on the value of the SIZE field (see [Table 1-33](#)). For example, if the SIZE field specifies a 256 kB page size, RPN[0:13] represents the physical page number and is used to form the physical address. RPN[14:21] is not used, and software must clear those bits to 0 when initializing the TLB entry. The remainder of the physical address is taken from the page-offset portion of the EA. If the page size is 256 kB, the 32-bit physical address is formed by concatenating RPN[0:13] with bits 14:31 of the effective address.

Prior to accessing physical memory, the MMU examines the TLB-entry access-control fields. These fields indicate whether the currently executing program is allowed to perform the requested memory access.

If access is allowed, the MMU checks the storage-attribute fields to determine how to access the page. The storage-attribute fields specify the caching policy for memory accesses.

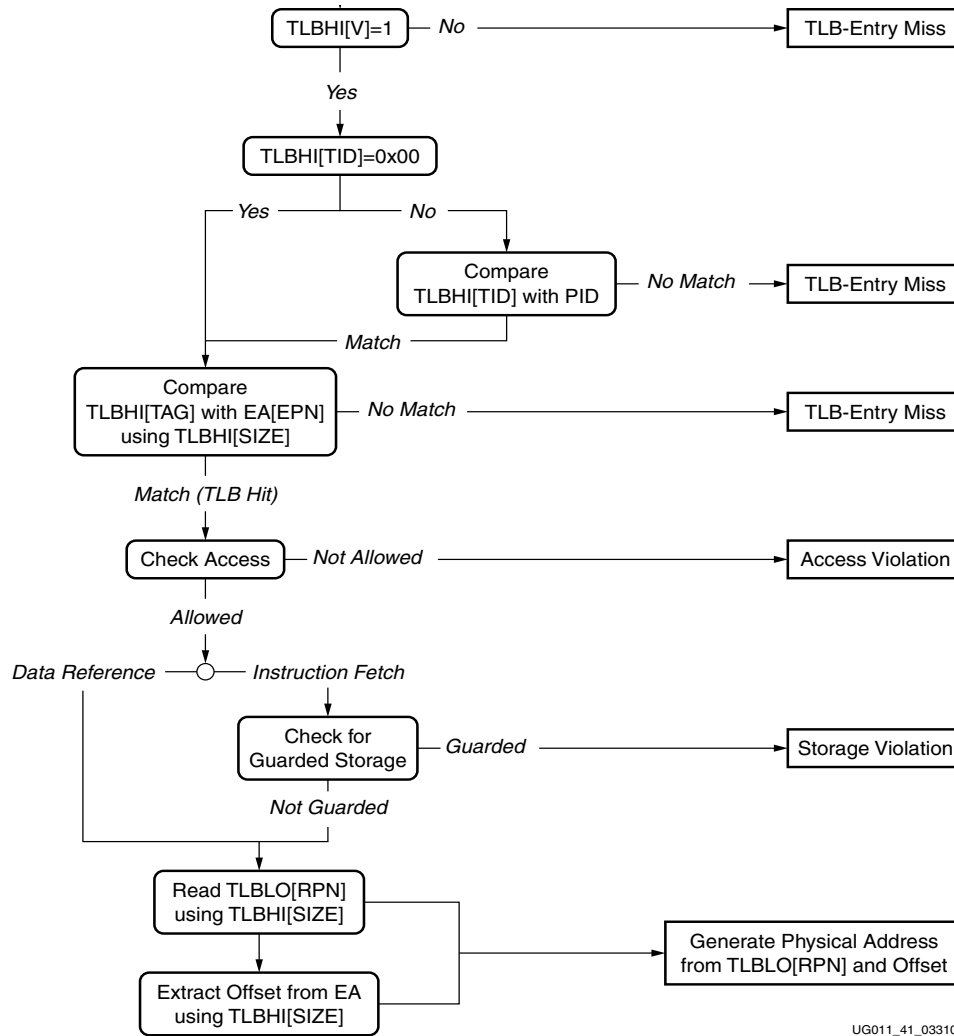
TLB Access Failures

A TLB-access failure causes an exception to occur. This interrupts execution of the instruction that caused the failure and transfers control to an interrupt handler to resolve the failure. A TLB access can fail for two reasons:

- A matching TLB entry was not found, resulting in a TLB miss
- A matching TLB entry was found, but access to the page was prevented by either the storage attributes or zone protection

When an interrupt occurs, the processor enters real mode by clearing MSR[VM] to 0. In real mode, all address translation and memory-protection checks performed by the MMU are disabled. After system software initializes the UTLB with page-translation entries, management of the MicroBlaze UTLB is usually performed using interrupt handlers running in real mode.

Table 1-19 diagrams the general process for examining a TLB entity.



UG011_41_033101

Figure 1-19: General Process for Examining a TLB Entry

The following sections describe the conditions under which exceptions occur due to TLB access failures.

Data-Storage Exception

When virtual mode is enabled, (MSR[VM]=1), a data-storage exception occurs when access to a page is not permitted for any of the following reasons:

- From user mode:
 - ◆ The TLB entry specifies a zone field that prevents access to the page ($ZPR[Zn]=00$). This applies to load and store instructions.
 - ◆ The TLB entry specifies a read-only page ($TLBLO[WR]=0$) that is not otherwise overridden by the zone field ($ZPR[Zn]$, 11). This applies to store instructions.
- From privileged mode:
 - ◆ The TLB entry specifies a read-only page ($TLBLO[WR]=0$) that is not otherwise overridden by the zone field ($ZPR[Zn]$, 10 and $ZPR[Zn]$, 11). This applies to store instructions.

Instruction-Storage Exception

When virtual mode is enabled, ($MSR[VM]=1$), an instruction-storage exception occurs when access to a page is not permitted for any of the following reasons:

- From user mode:
 - ◆ The TLB entry specifies a zone field that prevents access to the page ($ZPR[Zn]=00$).
 - ◆ The TLB entry specifies a non-executable page ($TLBLO[EX]=0$) that is not otherwise overridden by the zone field ($ZPR[Zn]$, 11).
 - ◆ The TLB entry specifies a guarded-storage page ($TLBLO[G]=1$).
- From privileged mode:
 - ◆ The TLB entry specifies a non-executable page ($TLBLO[EX]=0$) that is not otherwise overridden by the zone field ($ZPR[Zn]$, 10 and $ZPR[Zn]$, 11).
 - ◆ The TLB entry specifies a guarded-storage page ($TLBLO[G]=1$).

Data TLB-Miss Exception

When virtual mode is enabled ($MSR[VM]=1$) a data TLB-miss exception occurs if a valid, matching TLB entry was not found in the TLB (shadow and UTLB). Any load or store instruction can cause a data TLB-miss exception.

Instruction TLB-Miss Exception

When virtual mode is enabled ($MSR[VM]=1$) an instruction TLB-miss exception occurs if a valid, matching TLB entry was not found in the TLB (shadow and UTLB). Any instruction fetch can cause an instruction TLB-miss exception.

Access Protection

System software uses access protection to protect sensitive memory locations from improper access. System software can restrict memory accesses for both user-mode and privileged-mode software. Restrictions can be placed on reads, writes, and instruction fetches. Access protection is available when virtual protected mode is enabled.

Access control applies to instruction fetches, data loads, and data stores. The TLB entry for a virtual page specifies the type of access allowed to the page. The TLB entry also specifies a zone-protection field in the zone-protection register that is used to override the access controls specified by the TLB entry.

TLB Access-Protection Controls

Each TLB entry controls three types of access:

- **Process**—Processes are protected from unauthorized access by assigning a unique process ID (PID) to each process. When system software starts a user-mode application, it loads the PID for that application into the PID register. As the application executes, memory addresses are translated using only TLB entries with a TID field in Translation Look-Aside Buffer High (TLBHI) that matches the PID. This enables system software to restrict accesses for an application to a specific area in virtual memory.
A TLB entry with TID=0x00 represents a process-independent translation. Pages that are accessed globally by all processes should be assigned a TID value of 0x00.
- **Execution**—The processor executes instructions only if they are fetched from a virtual page marked as executable (TLBLO[EX]=1). Clearing TLBLO[EX] to 0 prevents execution of instructions fetched from a page, instead causing an instruction-storage interrupt (ISI) to occur. The ISI does not occur when the instruction is fetched, but instead occurs when the instruction is executed. This prevents speculatively fetched instructions that are later discarded (rather than executed) from causing an ISI.

The zone-protection register can override execution protection.

- **Read/Write**—Data is written only to virtual pages marked as writable (TLBLO[WR]=1). Clearing TLBLO[WR] to 0 marks a page as read-only. An attempt to write to a read-only page causes a data-storage interrupt (DSI) to occur.

The zone-protection register can override write protection.

TLB entries cannot be used to prevent programs from reading pages. In virtual mode, zone protection is used to read-protect pages. This is done by defining a no-access-allowed zone (ZPR[Zn] = 00) and using it to override the TLB-entry access protection. Only programs running in user mode can be prevented from reading a page. Privileged programs always have read access to a page.

Zone Protection

Zone protection is used to override the access protection specified in a TLB entry. Zones are an arbitrary grouping of virtual pages with common access protection. Zones can contain any number of pages specifying any combination of page sizes. There is no requirement for a zone to contain adjacent pages.

The zone-protection register (ZPR) is a 32-bit register used to specify the type of protection override applied to each of 16 possible zones. The protection override for a zone is encoded in the ZPR as a 2-bit field. The 4-bit zone-select field in a TLB entry (TLBLO[ZSEL]) selects one of the 16 zone fields from the ZPR (Z0–Z15). For example, zone Z5 is selected when ZSEL = 0101.

Changing a zone field in the ZPR applies a protection override across all pages in that zone. Without the ZPR, protection changes require individual alterations to each page translation entry within the zone.

UTLB Management

The UTLB serves as the interface between the processor MMU and memory-management software. System software manages the UTLB to tell the MMU how to translate virtual addresses into physical addresses. When a problem occurs due to a missing translation or an access violation, the MMU communicates the problem to system software using the exception mechanism. System software is responsible for providing interrupt handlers to correct these problems so that the MMU can proceed with memory translation.

Software reads and writes UTLB entries using the MFS and MTS instructions, respectively. These instructions use the TLBX register index (numbered 0 to 63) corresponding to one of the 64 entries

in the UTLB. The tag and data portions are read and written separately, so software must execute two MFS or MTS instructions to completely access an entry. The UTLB is searched for a specific translation using the TLBSX register. TLBSX locates a translation using an effective address and loads the corresponding UTLB index into the TLBX register.

Individual UTLB entries are invalidated using the MTS instruction to clear the valid bit in the tag portion of a TLB entry (TLBHI[V]).

Recording Page Access and Page Modification

Software management of virtual-memory poses several challenges:

- In a virtual-memory environment, software and data often consume more memory than is physically available. Some of the software and data pages must be stored outside physical memory, such as on a hard drive, when they are not used. Ideally, the most-frequently used pages stay in physical memory and infrequently used pages are stored elsewhere.
- When pages in physical-memory are replaced to make room for new pages, it is important to know whether the replaced (old) pages were modified. If they were modified, they must be saved prior to loading the replacement (new) pages. If the old pages were not modified, the new pages can be loaded without saving the old pages.
- A limited number of page translations are kept in the UTLB. The remaining translations must be stored in the page-translation table. When a translation is not found in the UTLB (due to a miss), system software must decide which UTLB entry to discard so that the missing translation can be loaded. It is desirable for system software to replace infrequently used translations rather than frequently used translations.

Solving the above problems in an efficient manner requires keeping track of page accesses and page modifications. MicroBlaze does not track page access and page modification in hardware. Instead, system software can use the TLB-miss exceptions and the data-storage exception to collect this information. As the information is collected, it can be stored in a data structure associated with the page-translation table.

Page-access information is used to determine which pages should be kept in physical memory and which are replaced when physical-memory space is required. System software can use the valid bit in the TLB entry (TLBHI[V]) to monitor page accesses. This requires page translations be initialized as not valid (TLBHI[V]=0) to indicate they have not been accessed. The first attempt to access a page causes a TLB-miss exception, either because the UTLB entry is marked not valid or because the page translation is not present in the UTLB. The TLB-miss handler updates the UTLB with a valid translation (TLBHI[V]=1). The set valid bit serves as a record that the page and its translation have been accessed. The TLB-miss handler can also record the information in a separate data structure associated with the page-translation entry.

Page-modification information is used to indicate whether an old page can be overwritten with a new page or the old page must first be stored to a hard disk. System software can use the write-protection bit in the TLB entry (TLBLO[WR]) to monitor page modification. This requires page translations be initialized as read-only (TLBLO[WR]=0) to indicate they have not been modified. The first attempt to write data into a page causes a data-storage exception, assuming the page has already been accessed and marked valid as described above. If software has permission to write into the page, the data-storage handler marks the page as writable (TLBLO[WR]=1) and returns. The set write-protection bit serves as a record that a page has been modified. The data-storage handler can also record this information in a separate data structure associated with the page-translation entry.

Tracking page modification is useful when virtual mode is first entered and when a new process is started.

Reset, Interrupts, Exceptions, and Break

MicroBlaze supports reset, interrupt, user exception, break, and hardware exceptions. The following section describes the execution flow associated with each of these events.

The relative priority starting with the highest is:

1. Reset
2. Hardware Exception
3. Non-maskable Break
4. Break
5. Interrupt
6. User Vector (Exception)

[Table 1-34](#) defines the memory address locations of the associated vectors and the hardware enforced register file locations for return addresses. Each vector allocates two addresses to allow full address range branching (requires an IMM followed by a BRAT instruction). The address range 0x28 to 0x4F is reserved for future software support by Xilinx. Allocating these addresses for user applications is likely to conflict with future releases of EDK support software.

Table 1-34: Vectors and Return Address Register File Location

Event	Vector Address	Register File Return Address
Reset	0x00000000 - 0x00000004	-
User Vector (Exception)	0x00000008 - 0x0000000C	Rx
Interrupt	0x00000010 - 0x00000014	R14
Break: Non-maskable hardware	0x00000018 - 0x0000001C	R16
Break: Hardware		
Break: Software		
Hardware Exception	0x00000020 - 0x00000024	R17 or BTR
Reserved by Xilinx for future use	0x00000028 - 0x0000004F	-

Reset

When a `Reset` or `Debug_Rst`⁽¹⁾ occurs, MicroBlaze flushes the pipeline and starts fetching instructions from the reset vector (address 0x0). Both external reset signals are active high and should be asserted for a minimum of 16 cycles.

Equivalent Pseudocode

```

PC ← 0x00000000
MSR ← C_RESET_MSR (see "MicroBlaze Core Configurability" in Chapter 2)
EAR ← 0; ESR ← 0; FSR ← 0
PID ← 0; ZPR ← 0; TLBX ← 0
    
```

1. Reset input controlled by the XMD debugger via MDM.

Hardware Exceptions

MicroBlaze can be configured to trap the following internal error conditions: illegal instruction, instruction and data bus error, and unaligned access. The divide by zero exception can only be enabled if the processor is configured with a hardware divider (`C_USE_DIV=1`). When configured with a hardware floating point unit (`C_USE_FPU>0`), it can also trap the following floating point specific exceptions: underflow, overflow, float division-by-zero, invalid operation, and denormalized operand error.

When configured with a hardware Memory Management Unit, it can also trap the following memory management specific exceptions: Illegal Instruction Exception, Data Storage Exception, Instruction Storage Exception, Data TLB Miss Exception, and Instruction TLB Miss Exception.

A hardware exception causes MicroBlaze to flush the pipeline and branch to the hardware exception vector (address `0x20`). The execution stage instruction in the exception cycle is not executed.

The exception also updates the general purpose register R17 in the following manner:

- For the MMU exceptions (Data Storage Exception, Instruction Storage Exception, Data TLB Miss Exception, Instruction TLB Miss Exception) the register R17 is loaded with the appropriate program counter value to re-execute the instruction causing the exception upon return. The value is adjusted to return to a preceding IMM instruction, if any. If the exception is caused by an instruction in a branch delay slot, the value is adjusted to return to the branch instruction, including adjustment for a preceding IMM instruction, if any.
- For all other exceptions the register R17 is loaded with the program counter value of the subsequent instruction, unless the exception is caused by an instruction in a branch delay slot. If the exception is caused by an instruction in a branch delay slot, the ESR[DS] bit is set. In this case the exception handler should resume execution from the branch target address stored in BTR.

The EE and EIP bits in MSR are automatically reverted when executing the RTED instruction.

The VM and UM bits in MSR are automatically reverted from VMS and UMS when executing the RTED, RTBD, and RTID instructions.

Exception Causes

- **Fast Simplex Link Exception**
The Fast Simplex Link (FSL) exception is caused by executing a `get` or `getd` instruction with the 'e' bit set to '1' when there is a control bit mismatch.
- **Instruction Bus Exception**
The instruction Processor Local Bus (PLB) exception is caused by an active error signal from the slave (`IPLB_MRdErr`) or timeout signal from the arbiter (`IPLB_MTimeout`). The instruction On-chip Peripheral Bus exception is caused by an active error signal from the slave (`IOPB_errAck`) or timeout signal from the arbiter (`IOPB_timeout`). The instructions side local memory (ILMB) and CacheLink (IXCL) interfaces cannot cause instruction bus exceptions.
- **Illegal Opcode Exception**
The illegal opcode exception is caused by an instruction with an invalid major opcode (bits 0 through 5 of instruction). Bits 6 through 31 of the instruction are not checked. Optional processor instructions are detected as illegal if not enabled. If the optional feature `C_OPCODE_0x0_ILLEGAL` is enabled, an illegal opcode exception is also caused if the instruction is equal to `0x00000000`.

- **Data Bus Exception**

The data Processor Local Bus exception is caused by an active error signal from the slave (DPLB_MRdErr or DPLB_MWrErr) or timeout signal from the arbiter (DPLB_MTimeout). The data On-chip Peripheral Bus exception is caused by an active error signal from the slave (DOPB_errAck) or timeout signal from the arbiter (DOPB_timeout). The data side local memory (DLMB) and CacheLink (DXCL) interfaces can not cause data bus exceptions.
- **Unaligned Exception**

The unaligned exception is caused by a word access where the address to the data bus has bits 30 or 31 set, or a half-word access with bit 31 set.
- **Divide by Zero Exception**

The divide-by-zero exception is caused by an integer division (idiv or idivu) where the divisor is zero.
- **FPU Exception**

An FPU exception is caused by an underflow, overflow, divide-by-zero, illegal operation, or denormalized operand occurring with a floating point instruction.

 - ◆ Underflow occurs when the result is denormalized.
 - ◆ Overflow occurs when the result is not-a-number (NaN).
 - ◆ The divide-by-zero FPU exception is caused by the rA operand to fdiv being zero when rB is not infinite.
 - ◆ Illegal operation is caused by a signaling NaN operand or by illegal infinite or zero operand combinations.
- **Privileged Instruction Exception**

The Privileged Instruction exception is caused by an attempt to execute a privileged instruction in User Mode.
- **Data Storage Exception**

The Data Storage exception is caused by an attempt to access data in memory that results in a memory-protection violation.
- **Instruction Storage Exception**

The Instruction Storage exception is caused by an attempt to access instructions in memory that results in a memory-protection violation.
- **Data TLB Miss Exception**

The Data TLB Miss exception is caused by an attempt to access data in memory, when a valid Translation Look-Aside Buffer entry is not present, and virtual protected mode is enabled.
- **Instruction TLB Miss Exception**

The Instruction TLB Miss exception is caused by an attempt to access instructions in memory, when a valid Translation Look-Aside Buffer entry is not present, and virtual protected mode is enabled.

Equivalent Pseudocode

```

ESR[DS] ← exception in delay slot
if ESR[DS] then
  BTR ← branch target PC
  if MMU exception then
    if branch preceeded by IMM then
      r17 ← PC - 8
    else
      r17 ← PC - 4
  else
    r17 ← invalid value
else if MMU exception then
  if instruction preceeded by IMM then
    r17 ← PC - 4
  else
    r17 ← PC
else
  r17 ← PC + 4
PC ← 0x00000020
MSR[EE] ← 0, MSR[EIP] ← 1
MSR[UMS] ← MSR[UM], MSR[UM] ← 0, MSR[VMS] ← MSR[VM], MSR[VM] ← 0
ESR[EC] ← exception specific value
ESR[ESS] ← exception specific value
EAR ← exception specific value
FSR ← exception specific value

```

Breaks

There are two kinds of breaks:

- Hardware (external) breaks
- Software (internal) breaks

Hardware Breaks

Hardware breaks are performed by asserting the external break signal (for example, the Ext_BRK and Ext_NM_BRK input ports). On a break, the instruction in the execution stage completes while the instruction in the decode stage is replaced by a branch to the break vector (address 0x18). The break return address (the PC associated with the instruction in the decode stage at the time of the break) is automatically loaded into general purpose register R16. MicroBlaze also sets the Break In Progress (BIP) flag in the Machine Status Register (MSR).

A normal hardware break (for example, the Ext_BRK input port) is only handled when there is no break in progress (for example, MSR[BIP] is set to 0). The Break In Progress flag disables interrupts. A non-maskable break (for example, the Ext_NM_BRK input port) is always handled immediately.

The BIP bit in the MSR is automatically cleared when executing the RTBD instruction.

Software Breaks

To perform a software break, use the `brk` and `brki` instructions. Refer to [Chapter 4, “MicroBlaze Instruction Set Architecture”](#) for detailed information on software breaks.

Latency

The time it takes MicroBlaze to enter a break service routine from the time the break occurs depends on the instruction currently in the execution stage and the latency to the memory storing the break vector.

Equivalent Pseudocode

```
r16 ← PC
PC ← 0x00000018
MSR[BIP] ← 1
MSR[UMS] ← MSR[UM], MSR[UM] ← 0, MSR[VMS] ← MSR[VM], MSR[VM] ← 0
```

Interrupt

MicroBlaze supports one external interrupt source (connected to the `Interrupt` input port). The processor only reacts to interrupts if the Interrupt Enable (IE) bit in the Machine Status Register (MSR) is set to 1. On an interrupt, the instruction in the execution stage completes while the instruction in the decode stage is replaced by a branch to the interrupt vector (address 0x10). The interrupt return address (the PC associated with the instruction in the decode stage at the time of the interrupt) is automatically loaded into general purpose register R14. In addition, the processor also disables future interrupts by clearing the IE bit in the MSR. The IE bit is automatically set again when executing the RTID instruction.

Interrupts are ignored by the processor if either of the break in progress (BIP) or exception in progress (EIP) bits in the MSR are set to 1.

Latency

The time it takes MicroBlaze to enter an Interrupt Service Routine (ISR) from the time an interrupt occurs, depends on the configuration of the processor and the latency of the memory controller storing the interrupt vectors. If MicroBlaze is configured to have a hardware divider, the largest latency happens when an interrupt occurs during the execution of a division instruction.

Equivalent Pseudocode

```
r14 ← PC
PC ← 0x00000010
MSR[IE] ← 0
MSR[UMS] ← MSR[UM], MSR[UM] ← 0, MSR[VMS] ← MSR[VM], MSR[VM] ← 0
```

User Vector (Exception)

The user exception vector is located at address 0x8. A user exception is caused by inserting a 'BRALID Rx, 0x8' instruction in the software flow. Although Rx could be any general purpose register, Xilinx recommends using R15 for storing the user exception return address, and to use the RTSD instruction to return from the user exception handler.

Pseudocode

```
rx ← PC
PC ← 0x00000008
MSR[UMS] ← MSR[UM], MSR[UM] ← 0, MSR[VMS] ← MSR[VM], MSR[VM] ← 0
```

Instruction Cache

Overview

MicroBlaze can be used with an optional instruction cache for improved performance when executing code that resides outside the LMB address range.

The instruction cache has the following features:

- Direct mapped (1-way associative)
- User selectable cacheable memory address range
- Configurable cache and tag size
- Caching over CacheLink (XCL) interface
- Option to use 4 or 8 word cache-line
- Cache on and off controlled using a bit in the MSR
- Optional WIC instruction to invalidate instruction cache lines

General Instruction Cache Functionality

When the instruction cache is used, the memory address space is split into two segments: a cacheable segment and a non-cacheable segment. The cacheable segment is determined by two parameters: `C_ICACHE_BASEADDR` and `C_ICACHE_HIGHADDR`. All addresses within this range correspond to the cacheable address segment. All other addresses are non-cacheable.

The cacheable instruction address consists of two parts: the cache address, and the tag address. The MicroBlaze instruction cache can be configured from 64 bytes to 64 kB. This corresponds to a cache address of between 6 and 16 bits. The tag address together with the cache address should match the full address of cacheable memory. When selecting cache sizes below 2 kB, distributed RAM is used to implement the Tag RAM and Instruction RAM.

For example: in a MicroBlaze configured with `C_ICACHE_BASEADDR= 0x00300000`, `C_ICACHE_HIGHADDR=0x0030ffff`, `C_CACHE_BYTE_SIZE=4096`, and `C_ICACHE_LINELEN=8`; the cacheable memory of 64 kB uses 16 bits of byte address, and the 4 kB cache uses 12 bits of byte address, thus the required address tag width is: $16-12=4$ bits. The total number of block RAM primitives required in this configuration is: 2 RAMB16 for storing the 1024 instruction words, and 1 RAMB16 for 128 cache line entries, each consisting of: 4 bits of tag, 8 word-valid bits, 1 line-valid bit. In total 3 RAMB16 primitives.

[Figure 1-20, page 64](#) shows the organization of Instruction Cache.

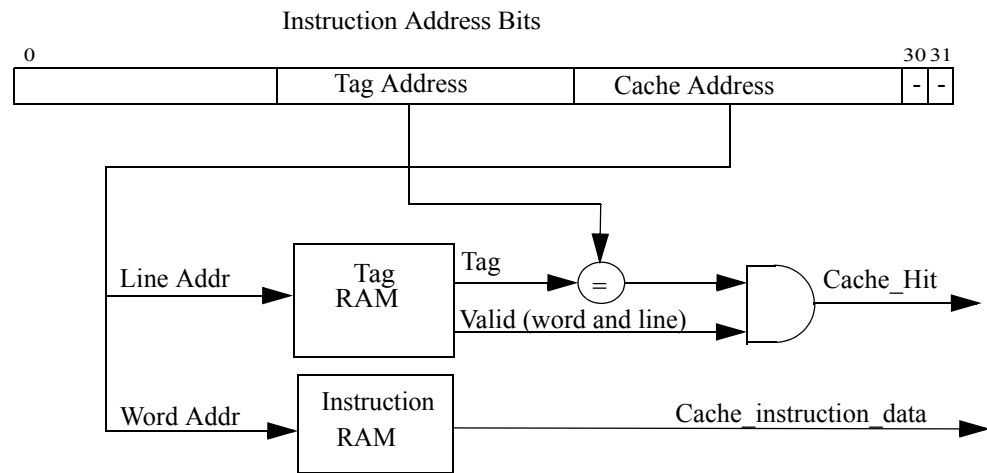


Figure 1-20: Instruction Cache Organization

Instruction Cache Operation

For every instruction fetched, the instruction cache detects if the instruction address belongs to the cacheable segment. If the address is non-cacheable, the cache controller ignores the instruction and lets the PLB, OPB or LMB complete the request. If the address is cacheable, a lookup is performed on the tag memory to check if the requested address is currently cached. The lookup is successful if: the word and line valid bits are set, and the tag address matches the instruction address tag segment. On a cache miss, the cache controller requests the new instruction over the instruction CacheLink (IXCL) interface, and waits for the memory controller to return the associated cache line.

Instruction Cache Software Support

MSR Bit

The ICE bit in the MSR provides software control to enable and disable caches.

The contents of the cache are preserved by default when the cache is disabled. You can invalidate cache lines using the WIC instruction or using the hardware debug logic of MicroBlaze.

WIC Instruction

The optional WIC instruction (`C_ALLOW_ICACHE_WR=1`) is used to invalidate cache lines in the instruction cache from an application. For a detailed description, refer to [Chapter 4, “MicroBlaze Instruction Set Architecture”](#). The cache must be disabled (`MSR[ICE]=0`) when the instruction is executed.

Data Cache

Overview

MicroBlaze can be used with an optional data cache for improved performance. The cached memory range must not include addresses in the LMB address range.

The data cache has the following features

- Direct mapped (1-way associative)
- Write-through
- User selectable cacheable memory address range
- Configurable cache size and tag size
- Caching over CacheLink (XCL) interface
- Option to use 4 or 8 word cache-lines
- Cache on and off controlled using a bit in the MSR
- Optional WDC instruction to invalidate data cache lines

General Data Cache Functionality

When the data cache is used, the memory address space is split into two segments: a cacheable segment and a non-cacheable segment. The cacheable area is determined by two parameters: `C_DCACHE_BASEADDR` and `C_DCACHE_HIGHADDR`. All addresses within this range correspond to the cacheable address space. All other addresses are non-cacheable.

The cacheable data address consists of two parts: the cache address, and the tag address. The MicroBlaze data cache can be configured from 64 bytes to 64 kB. This corresponds to a cache address of between 6 and 16 bits. The tag address together with the cache address should match the full address of cacheable memory. When selecting cache sizes below 2 kB, distributed RAM is used to implement the Tag RAM and Data RAM.

Figure 1-20 shows the Data Cache Organization.

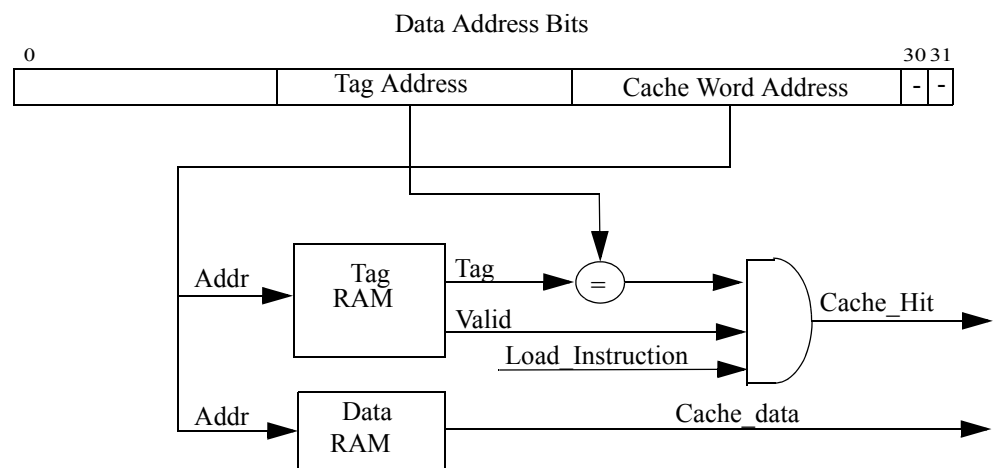


Figure 1-21: Data Cache Organization

For example, in a MicroBlaze configured with `C_ICACHE_BASEADDR= 0x00400000`, `C_ICACHE_HIGHADDR=0x00403fff`, `C_CACHE_BYTE_SIZE=2048`, and `C_ICACHE_LINELEN=4`; the cacheable memory of 16 kB uses 14 bits of byte address, and the 2 kB cache uses 11 bits of byte address, thus the required address tag width is $14-11=3$ bits. The total number of block RAM primitives required in this configuration is 1 RAMB16 for storing the 512 instruction words, and 1 RAMB16 for 128 cache line entries, each consisting of 3 bits of tag, 4 word-valid bits, 1 line-valid bit. In total, 2 RAMB16 primitives.

Data Cache Operation

The MicroBlaze data cache implements a write-through protocol. Provided that the cache is enabled, a store to an address within the cacheable range generates an equivalent byte, halfword, or word write over the data CacheLink (DXCL) to external memory. The write also updates the cached data if the target address word is in the cache (for example, the write is a cache-hit). A write cache-miss does not load the associated cache line into the cache.

Provided that the cache is enabled a load from an address within the cacheable range triggers a check to determine if the requested data is currently cached. If it is (for example, on a cache-hit) the requested data is retrieved from the cache. If not (for example, on a cache-miss) the address is requested over data CacheLink (DXCL), and the processor pipeline stalls until the cache line associated to the requested address is returned from the external memory controller.

Data Cache Software Support

MSR Bit

The DCE bit in the MSR controls whether or not the cache is enabled. When disabling caches the user must ensure that all the prior writes within the cacheable range have been completed in external memory before reading back over PLB or OPB. This can be done by writing to a semaphore immediately before turning off caches, and then in a loop poll until it has been written.

The contents of the cache are preserved when the cache is disabled.

WDC Instruction

The optional WDC instruction (`C_ALLOW_DCACHE_WR=1`) is used to invalidate cache lines in the data cache from an application. For a detailed description, please refer to [Chapter 4, “MicroBlaze Instruction Set Architecture”](#).

Floating Point Unit (FPU)

Overview

The MicroBlaze floating point unit is based on the [IEEE 754 standard](#):

- Uses IEEE 754 single precision floating point format, including definitions for infinity, not-a-number (NaN), and zero
- Supports addition, subtraction, multiplication, division, comparison, conversion and square root instructions
- Implements round-to-nearest mode
- Generates sticky status bits for: underflow, overflow, and invalid operation

For improved performance, the following non-standard simplifications are made:

- Denormalized⁽¹⁾ operands are not supported. A hardware floating point operation on a denormalized number returns a quiet NaN and sets the denormalized operand error bit in FSR; see "Floating Point Status Register (FSR)" on page 30
- A denormalized result is stored as a signed 0 with the underflow bit set in FSR. This method is commonly referred to as Flush-to-Zero (FTZ)
- An operation on a quiet NaN returns the fixed NaN: 0xFFC00000, rather than one of the NaN operands
- Overflow as a result of a floating point operation always returns signed ∞ , even when the exception is trapped

Format

An IEEE 754 single precision floating point number is composed of the following three fields:

1. 1-bit *sign*
2. 8-bit biased *exponent*
3. 23-bit *fraction* (a.k.a. mantissa or significand)

The fields are stored in a 32 bit word as defined in [Figure 1-22](#):

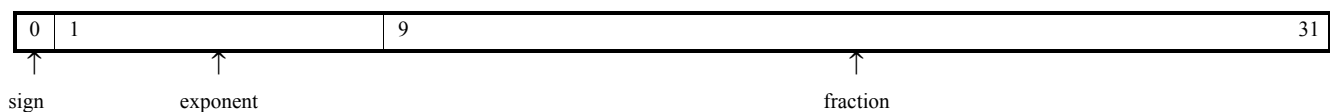


Figure 1-22: IEEE 754 Single Precision Format

The value of a floating point number v in MicroBlaze has the following interpretation:

1. If $exponent = 255$ and $fraction \neq 0$, then $v = NaN$, regardless of the *sign* bit
2. If $exponent = 255$ and $fraction = 0$, then $v = (-1)^{sign} * \infty$
3. If $0 < exponent < 255$, then $v = (-1)^{sign} * 2^{(exponent-127)} * (1.fraction)$
4. If $exponent = 0$ and $fraction \neq 0$, then $v = (-1)^{sign} * 2^{-126} * (0.fraction)$
5. If $exponent = 0$ and $fraction = 0$, then $v = (-1)^{sign} * 0$

1. Numbers that are so close to 0, that they cannot be represented with full precision, for example, any number n that falls in the following ranges: $(1.17549 * 10^{-38} > n > 0)$, or $(0 > n > -1.17549 * 10^{-38})$

For practical purposes only 3 and 5 are useful, while the others all represent either an error or numbers that can no longer be represented with full precision in a 32 bit format.

Rounding

The MicroBlaze FPU only implements the default rounding mode, “Round-to-nearest”, specified in IEEE 754. By definition, the result of any floating point operation should return the nearest single precision value to the infinitely precise result. If the two nearest representable values are equally near, then the one with its least significant bit zero is returned.

Operations

All MicroBlaze FPU operations use the processors general purpose registers rather than a dedicated floating point register file, see “[General Purpose Registers](#)”.

Arithmetic

The FPU implements the following floating point operations:

- addition, fadd
- subtraction, fsub
- multiplication, fmul
- division, fdiv
- square root, fsqrt (available if `C_USE_FPU = 2`)

Comparison

The FPU implements the following floating point comparisons:

- compare less-than, fcmp.lt
- compare equal, fcmp.eq
- compare less-or-equal, fcmp.le
- compare greater-than, fcmp.gt
- compare not-equal, fcmp.ne
- compare greater-or-equal, fcmp.ge
- compare unordered, fcmp.un (used for NaN)

Conversion

The FPU implements the following conversions (available if `C_USE_FPU = 2`):

- convert from signed integer to floating point, flt
- convert from floating point to signed integer, fint

Exceptions

The floating point unit uses the regular hardware exception mechanism in MicroBlaze. When enabled, exceptions are thrown for all the IEEE standard conditions: underflow, overflow, divide-by-zero, and illegal operation, as well as for the MicroBlaze specific exception: denormalized operand error.

A floating point exception inhibits the write to the destination register (Rd). This allows a floating point exception handler to operate on the uncorrupted register file.

Fast Simplex Link (FSL)

MicroBlaze can be configured with up to 16 Fast Simplex Link (FSL) interfaces, each consisting of one input and one output port. The FSL channels are dedicated uni-directional point-to-point data streaming interfaces. For detailed information on the FSL interface, please refer to the FSL Bus data sheet (DS449).

The FSL interfaces on MicroBlaze are 32 bits wide. A separate bit indicates whether the sent/received word is of control or data type. The get instruction in the MicroBlaze ISA is used to transfer information from an FSL port to a general purpose register. The put instruction is used to transfer data in the opposite direction. Both instructions come in 4 flavors: blocking data, non-blocking data, blocking control, and non-blocking control. For a detailed description of the get and put instructions, please refer to [Chapter 4, “MicroBlaze Instruction Set Architecture”](#).

Hardware Acceleration using FSL

Each FSL provides a low latency dedicated interface to the processor pipeline. Thus they are ideal for extending the processors execution unit with custom hardware accelerators. A simple example is illustrated in [Figure 1-23](#).

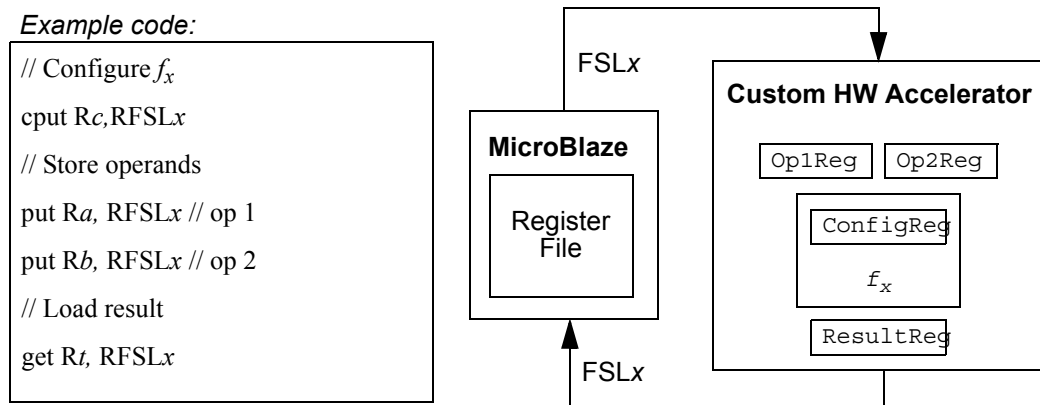


Figure 1-23: FSL Used with HW Accelerated Function f_x

This method is similar to extending the ISA with custom instructions, but has the benefit of not making the overall speed of the processor pipeline dependent on the custom function. Also, there are no additional requirements on the software tool chain associated with this type of functional extension.

Debug and Trace

Debug Overview

MicroBlaze features a debug interface to support JTAG based software debugging tools (commonly known as BDM or Background Debug Mode debuggers) like the Xilinx Microprocessor Debug (XMD) tool. The debug interface is designed to be connected to the Xilinx Microprocessor Debug Module (MDM) core, which interfaces with the JTAG port of Xilinx FPGAs. Multiple MicroBlaze instances can be interfaced with a single MDM to enable multiprocessor debugging. The debugging features include:

- Configurable number of hardware breakpoints and watchpoints and unlimited software breakpoints
- External processor control enables debug tools to stop, reset, and single step MicroBlaze
- Read from and write to: memory, general purpose registers, and special purpose register, except EAR, EDR, ESR, BTR and PVR0 - PVR11, which can only be read
- Support for multiple processors
- Write to instruction and data caches

Trace Overview

The MicroBlaze trace interface exports a number of internal state signals for performance monitoring and analysis. Xilinx recommends that users only use the trace interface through Xilinx developed analysis cores. This interface is not guaranteed to be backward compatible in future releases of MicroBlaze.

MicroBlaze Signal Interface Description

This chapter describes the types of signal interfaces that can be used to connect MicroBlaze™. This chapter contains the following sections:

- “Overview”
- “MicroBlaze I/O Overview”
- “On-Chip Peripheral Bus (OPB) Interface Description”
- “Local Memory Bus (LMB) Interface Description”
- “Fast Simplex Link (FSL) Interface Description”
- “Xilinx CacheLink (XCL) Interface Description”
- “Debug Interface Description”
- “Trace Interface Description”
- “MicroBlaze Core Configurability”

Overview

The MicroBlaze core is organized as a Harvard architecture with separate bus interface units for data and instruction accesses. The following three memory interfaces are supported: Local Memory Bus (LMB), the IBM Processor Local Bus (PLB) or the IBM On-chip Peripheral Bus (OPB), and Xilinx® CacheLink (XCL). The LMB provides single-cycle access to on-chip dual-port block RAM. The PLB and OPB interfaces provide a connection to both on-chip and off-chip peripherals and memory. The CacheLink interface is intended for use with specialized external memory controllers. MicroBlaze also supports up to 16 Fast Simplex Link (FSL) ports, each with one master and one slave FSL interface.

Features

MicroBlaze can be configured with the following bus interfaces:

- A 32-bit version of the PLB V4.6 interface (see IBM’s *128-Bit Processor Local Bus Architectural Specifications, Version 4.6*).
- A 32-bit version of the OPB V2.0 bus interface (see IBM’s *64-Bit On-Chip Peripheral Bus, Architectural Specifications, Version 2.0*)
- LMB provides simple synchronous protocol for efficient block RAM transfers
- FSL provides a fast non-arbitrated streaming communication mechanism
- XCL provides a fast slave-side arbitrated streaming interface between caches and external memory controllers
- Debug interface for use with the Microprocessor Debug Module (MDM) core
- Trace interface for performance analysis

MicroBlaze I/O Overview

The core interfaces shown in Figure 2-1 and the following Table 2-1 are defined as follows:

- DPLB:** Data interface, Processor LocalBus
- DOPB:** Data interface, On-chip Peripheral Bus
- DLMB:** Data interface, Local Memory Bus (BRAM only)
- IPLB:** Instruction interface, Processor Local Bus
- IOPB:** Instruction interface, On-chip Peripheral Bus
- ILMB:** Instruction interface, Local Memory Bus (BRAM only)
- MFSL 0..15:** FSL master interfaces
- SFSL 0..15:** FSL slave interfaces
- IXCL:** Instruction side Xilinx CacheLink interface (FSL master/slave pair)
- DXCL:** Data side Xilinx CacheLink interface (FSL master/slave pair)
- Core:** Miscellaneous signals for: clock, reset, debug, and trace

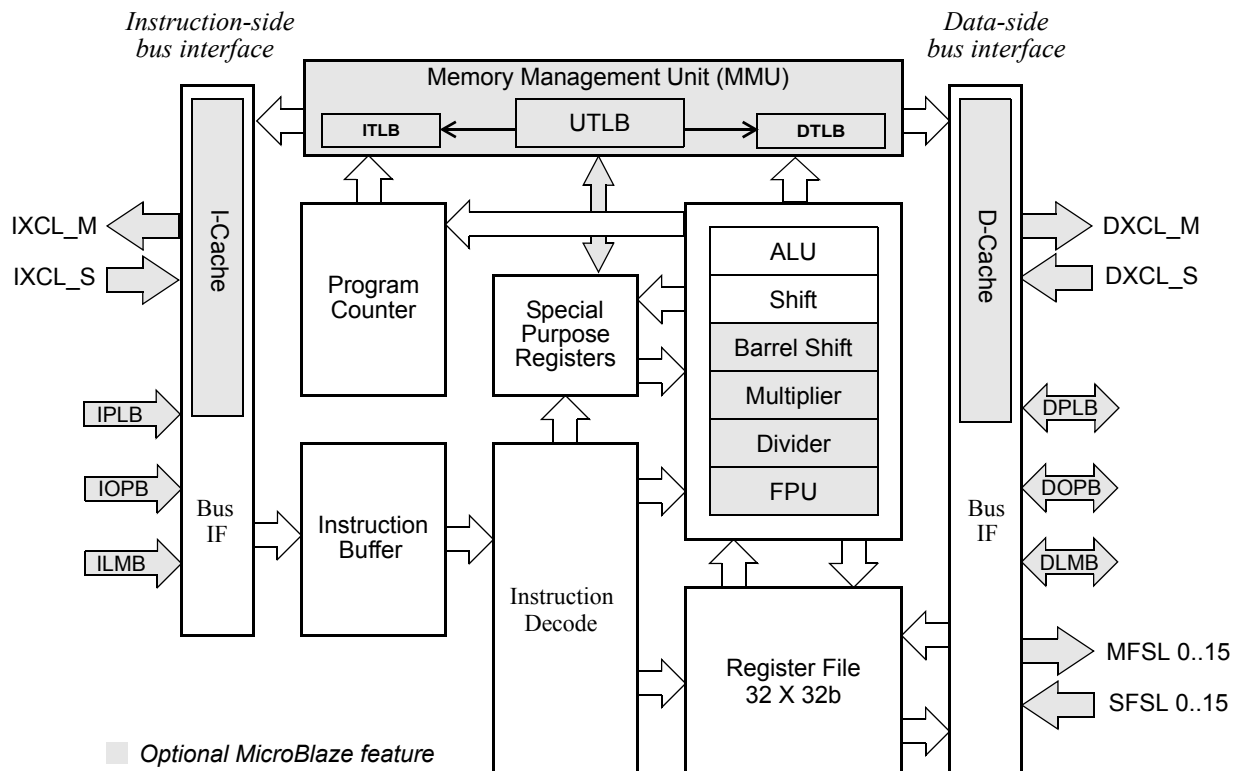


Figure 2-1: MicroBlaze Core Block Diagram

Table 2-1: Summary of MicroBlaze Core I/O

Signal	Interface	I/O	Description
DM_ABus [0:31]	DOPB	O	Data interface OPB address bus
DM_BE [0:3]	DOPB	O	Data interface OPB byte enables
DM_busLock	DOPB	O	Data interface OPB bus lock
DM_DBus [0:31]	DOPB	O	Data interface OPB write data bus
DM_request	DOPB	O	Data interface OPB bus request
DM_RNW	DOPB	O	Data interface OPB read, not write
DM_select	DOPB	O	Data interface OPB select
DM_seqAddr	DOPB	O	Data interface OPB sequential address
DOPB_DBus [0:31]	DOPB	I	Data interface OPB read data bus
DOPB_errAck	DOPB	I	Data interface OPB error acknowledge
DOPB_MGrant	DOPB	I	Data interface OPB bus grant
DOPB_retry	DOPB	I	Data interface OPB bus cycle retry
DOPB_timeout	DOPB	I	Data interface OPB timeout error
DOPB_xferAck	DOPB	I	Data interface OPB transfer acknowledge
IM_ABus [0:31]	IOPB	O	Instruction interface OPB address bus
IM_BE [0:3]	IOPB	O	Instruction interface OPB byte enables
IM_busLock	IOPB	O	Instruction interface OPB bus lock
IM_DBus [0:31]	IOPB	O	Instruction interface OPB write data bus (always 0x00000000)
IM_request	IOPB	O	Instruction interface OPB bus request
IM_RNW	IOPB	O	Instruction interface OPB read, not write (tied to IM_select)
IM_select	IOPB	O	Instruction interface OPB select
IM_seqAddr	IOPB	O	Instruction interface OPB sequential address
IOPB_DBus [0:31]	IOPB	I	Instruction interface OPB read data bus
IOPB_errAck	IOPB	I	Instruction interface OPB error acknowledge
IOPB_MGrant	IOPB	I	Instruction interface OPB bus grant
IOPB_retry	IOPB	I	Instruction interface OPB bus cycle retry
IOPB_timeout	IOPB	I	Instruction interface OPB timeout error
IOPB_xferAck	IOPB	I	Instruction interface OPB transfer acknowledge

Table 2-1: Summary of MicroBlaze Core I/O (Continued)

Signal	Interface	I/O	Description
DPLB_M_Abort	DPLB	O	Data Interface PLB abort bus request indicator
DPLB_M_ABus	DPLB	O	Data Interface PLB address bus
DPLB_M_UABus	DPLB	O	Data Interface PLB upper address bus
DPLB_M_BE	DPLB	O	Data Interface PLB byte enables
DPLB_M_busLock	DPLB	O	Data Interface PLB bus lock
DPLB_M_lockErr	DPLB	O	Data Interface PLB lock error indicator
DPLB_M_MSize	DPLB	O	Data Interface PLB master data bus size
DPLB_M_priority	DPLB	O	Data Interface PLB bus request priority
DPLB_M_rdBurst	DPLB	O	Data Interface PLB burst read transfer indicator
DPLB_M_request	DPLB	O	Data Interface PLB bus request
DPLB_M_RNW	DPLB	O	Data Interface PLB read/not write
DPLB_M_size	DPLB	O	Data Interface PLB transfer size
DPLB_M_TAttribute	DPLB	O	Data Interface PLB Transfer Attribute bus
DPLB_M_type	DPLB	O	Data Interface PLB transfer type
DPLB_M_wrBurst	DPLB	O	Data Interface PLB burst write transfer indicator
DPLB_M_wrDBus	DPLB	O	Data Interface PLB write data bus
DPLB_MBusy	DPLB	I	Data Interface PLB slave busy indicator
DPLB_MRdErr	DPLB	I	Data Interface PLB slave read error indicator
DPLB_MWrErr	DPLB	I	Data Interface PLB slave write error indicator
DPLB_MIRQ	DPLB	I	Data Interface PLB slave interrupt indicator
DPLB_MWrBTerm	DPLB	I	Data Interface PLB terminate write burst indicator
DPLB_MWrDAck	DPLB	I	Data Interface PLB write data acknowledge
DPLB_MAddrAck	DPLB	I	Data Interface PLB address acknowledge
DPLB_MMRdBTerm	DPLB	I	Data Interface PLB terminate read burst indicator
DPLB_MRdDAck	DPLB	I	Data Interface PLB read data acknowledge
DPLB_MRdDBus	DPLB	I	Data Interface PLB read data bus
DPLB_MRdWdAddr	DPLB	I	Data Interface PLB read word address
DPLB_MRearbitrate	DPLB	I	Data Interface PLB bus rearbitrate indicator

Table 2-1: Summary of MicroBlaze Core I/O (Continued)

Signal	Interface	I/O	Description
DPLB_MSSize	DPLB	I	Data Interface PLB slave data bus size
DPLB_MTimeout	DPLB	I	Data Interface PLB bus timeout
IPLB_M_Abort	IPLB	O	Instruction Interface PLB abort bus request indicator
IPLB_M_ABus	IPLB	O	Instruction Interface PLB address bus
IPLB_M_UABus	IPLB	O	Instruction Interface PLB upper address bus
IPLB_M_BE	IPLB	O	Instruction Interface PLB byte enables
IPLB_M_busLock	IPLB	O	Instruction Interface PLB bus lock
IPLB_M_lockErr	IPLB	O	Instruction Interface PLB lock error indicator
IPLB_M_MSize	IPLB	O	Instruction Interface PLB master data bus size
IPLB_M_priority	IPLB	O	Instruction Interface PLB bus request priority
IPLB_M_rdBurst	IPLB	O	Instruction Interface PLB burst read transfer indicator
IPLB_M_request	IPLB	O	Instruction Interface PLB bus request
IPLB_M_RNW	IPLB	O	Instruction Interface PLB read/not write
IPLB_M_size	IPLB	O	Instruction Interface PLB transfer size
IPLB_M_TAttribute	IPLB	O	Instruction Interface PLB Transfer Attribute bus
IPLB_M_type	IPLB	O	Instruction Interface PLB transfer type
IPLB_M_wrBurst	IPLB	O	Instruction Interface PLB burst write transfer indicator
IPLB_M_wrDBus	IPLB	O	Instruction Interface PLB write data bus
IPLB_MBusy	IPLB	I	Instruction Interface PLB slave busy indicator
IPLB_MRdErr	IPLB	I	Instruction Interface PLB slave read error indicator
IPLB_MWrErr	IPLB	I	Instruction Interface PLB slave write error indicator
IPLB_MIRQ	IPLB	I	Instruction Interface PLB slave interrupt indicator
IPLB_MWrBTerm	IPLB	I	Instruction Interface PLB terminate write burst indicator
IPLB_MWrDAck	IPLB	I	Instruction Interface PLB write data acknowledge

Table 2-1: Summary of MicroBlaze Core I/O (Continued)

Signal	Interface	I/O	Description
IPLB_MAddrAck	IPLB	I	Instruction Interface PLB address acknowledge
IPLB_MMRdBTerm	IPLB	I	Instruction Interface PLB terminate read burst indicator
IPLB_MRdDAck	IPLB	I	Instruction Interface PLB read data acknowledge
IPLB_MRdDBus	IPLB	I	Instruction Interface PLB read data bus
IPLB_MRdWdAddr	IPLB	I	Instruction Interface PLB read word address
IPLB_MRearbitrate	IPLB	I	Instruction Interface PLB bus rearbitrate indicator
IPLB_MSSize	IPLB	I	Instruction Interface PLB slave data bus size
IPLB_MTimeout	IPLB	I	Instruction Interface PLB bus timeout
Data_Addr[0:31]	DLMB	O	Data interface LMB address bus
Byte_Enable[0:3]	DLMB	O	Data interface LMB byte enables
Data_Write[0:31]	DLMB	O	Data interface LMB write data bus
D_AS	DLMB	O	Data interface LMB address strobe
Read_Strobe	DLMB	O	Data interface LMB read strobe
Write_Strobe	DLMB	O	Data interface LMB write strobe
Data_Read[0:31]	DLMB	I	Data interface LMB read data bus
DReady	DLMB	I	Data interface LMB data ready
Instr_Addr[0:31]	ILMB	O	Instruction interface LMB address bus
I_AS	ILMB	O	Instruction interface LMB address strobe
IFetch	ILMB	O	Instruction interface LMB instruction fetch
Instr[0:31]	ILMB	I	Instruction interface LMB read data bus
IReady	ILMB	I	Instruction interface LMB data ready
FSL0_M .. FSL15_M	MFSL	O	Master interface to output FSL channels
FSL0_S .. FSL15_S	SFSL	I	Slave interface to input FSL channels
ICache_FSL_in...	IXCL_S	IO	Instruction side CacheLink FSL slave interface
ICache_FSL_out...	IXCL_M	IO	Instruction side CacheLink FSL master interface
DCache_FSL_in...	DXCL_S	IO	Data side CacheLink FSL slave interface
DCache_FSL_out...	DXCL_M	IO	Data side CacheLink FSL master interface
Interrupt	Core	I	Interrupt

Table 2-1: Summary of MicroBlaze Core I/O (Continued)

Signal	Interface	I/O	Description
Reset	Core	I	Core reset, active high. Should be held for at least 1 Clk clock cycle.
Mb_Reset	Core	I	Core reset, active high. Should be held for at least 1 Clk clock cycle.
Clk	Core	I	Clock ¹
Ext_BRK	Core	I	Break signal from OPB JTAG UART
Ext_NM_BRK	Core	I	Non-maskable break signal from OPB JTAG UART
MB_Halted	Core	O	Pipeline is halted
Dbg_...	Core	IO	Debug signals from OPB MDM. See Table 2-9 for details.
Trace_...	Core	O	Trace signals for real time HW analysis. See Table 2-10 for details.

1. MicroBlaze is a synchronous design clocked with the Clk signal, except for hardware debug logic, which is clocked with the Dbg_Clk signal. If hardware debug logic is not used, there is no minimum frequency limit for Clk. However, if hardware debug logic is used, there are signals transferred between the two clock regions. In this case Clk must have a higher frequency than Dbg_Clk.

Processor Local Bus (PLB) Interface Description

The MicroBlaze PLB interfaces are implemented as byte-enable capable 32-bit masters. Please refer to the *PLBV46 Interconnect and Interfaces* document for details.

On-Chip Peripheral Bus (OPB) Interface Description

The MicroBlaze OPB interfaces are implemented as byte-enable capable masters. Please refer to the *OPB Usage in Xilinx FPGA* document for details.

Local Memory Bus (LMB) Interface Description

The LMB is a synchronous bus used primarily to access on-chip block RAM. It uses a minimum number of control signals and a simple protocol to ensure that local block RAM are accessed in a single clock cycle. LMB signals and definitions are shown in the following table. All LMB signals are active high.

LMB Signal Interface

Table 2-2: LMB Bus Signals

Signal	Data Interface	Instruction Interface	Type	Description
Addr[0:31]	Data_Addr[0:31]	Instr_Addr[0:31]	O	Address bus
Byte_Enable[0:3]	Byte_Enable[0:3]	<i>not used</i>	O	Byte enables
Data_Write[0:31]	Data_Write[0:31]	<i>not used</i>	O	Write data bus
AS	D_AS	I_AS	O	Address strobe
Read_Strobe	Read_Strobe	IFetch	O	Read in progress
Write_Strobe	Write_Strobe	<i>not used</i>	O	Write in progress
Data_Read[0:31]	Data_Read[0:31]	Instr[0:31]	I	Read data bus
Ready	DReady	IReady	I	Ready for next transfer
Clk	Clk	Clk	I	Bus clock

Addr[0:31]

The address bus is an output from the core and indicates the memory address that is being accessed by the current transfer. It is valid only when AS is high. In multicycle accesses (accesses requiring more than one clock cycle to complete), Addr[0:31] is valid only in the first clock cycle of the transfer.

Byte_Enable[0:3]

The byte enable signals are outputs from the core and indicate which byte lanes of the data bus contain valid data. Byte_Enable[0:3] is valid only when AS is high. In multicycle accesses (accesses requiring more than one clock cycle to complete), Byte_Enable[0:3] is valid only in the first clock cycle of the transfer. Valid values for Byte_Enable[0:3] are shown in the following table:

Table 2-3: Valid Values for Byte_Enable[0:3]

Byte_Enable[0:3]	Byte Lanes Used			
	Data[0:7]	Data[8:15]	Data[16:23]	Data[24:31]
0000				
0001				x
0010			x	
0100		x		
1000	x			
0011			x	x

Table 2-3: Valid Values for Byte_Enable[0:3] (Continued)

Byte_Enable[0:3]	Byte Lanes Used			
	Data[0:7]	Data[8:15]	Data[16:23]	Data[24:31]
1100	x	x		
1111	x	x	x	x

Data_Write[0:31]

The write data bus is an output from the core and contains the data that is written to memory. It becomes valid when AS is high and goes invalid in the clock cycle after Ready is sampled high. Only the byte lanes specified by Byte_Enable[0:3] contain valid data.

AS

The address strobe is an output from the core and indicates the start of a transfer and qualifies the address bus and the byte enables. It is high only in the first clock cycle of the transfer, after which it goes low and remains low until the start of the next transfer.

Read_Strobe

The read strobe is an output from the core and indicates that a read transfer is in progress. This signal goes high in the first clock cycle of the transfer, and remains high until the clock cycle after Ready is sampled high. If a new read transfer is started in the clock cycle after Ready is high, then Read_Strobe remains high.

Write_Strobe

The write strobe is an output from the core and indicates that a write transfer is in progress. This signal goes high in the first clock cycle of the transfer, and remains high until the clock cycle after Ready is sampled high. If a new write transfer is started in the clock cycle after Ready is high, then Write_Strobe remains high.

Data_Read[0:31]

The read data bus is an input to the core and contains data read from memory. Data_Read[0:31] is valid on the rising edge of the clock when Ready is high.

Ready

The Ready signal is an input to the core and indicates completion of the current transfer and that the next transfer can begin in the following clock cycle. It is sampled on the rising edge of the clock. For reads, this signal indicates the Data_Read[0:31] bus is valid, and for writes it indicates that the Data_Write[0:31] bus has been written to local memory.

Clk

All operations on the LMB are synchronous to the MicroBlaze core clock.

LMB Transactions

The following diagrams provide examples of LMB bus operations.

Generic Write Operation

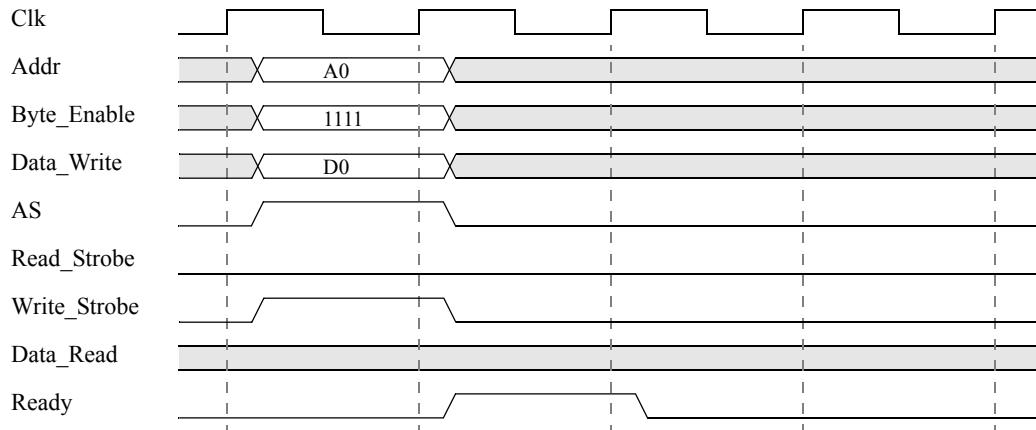


Figure 2-2: LMB Generic Write Operation

Generic Read Operation

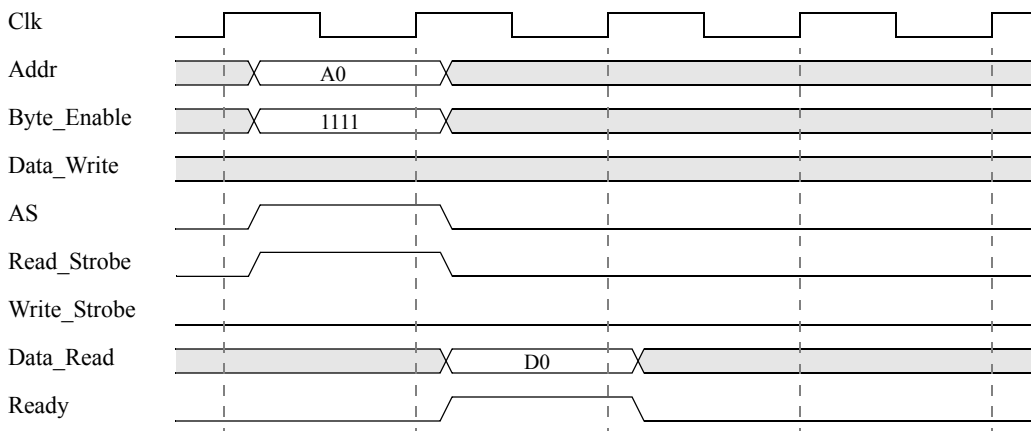


Figure 2-3: LMB Generic Read Operation

Back-to-Back Write Operation

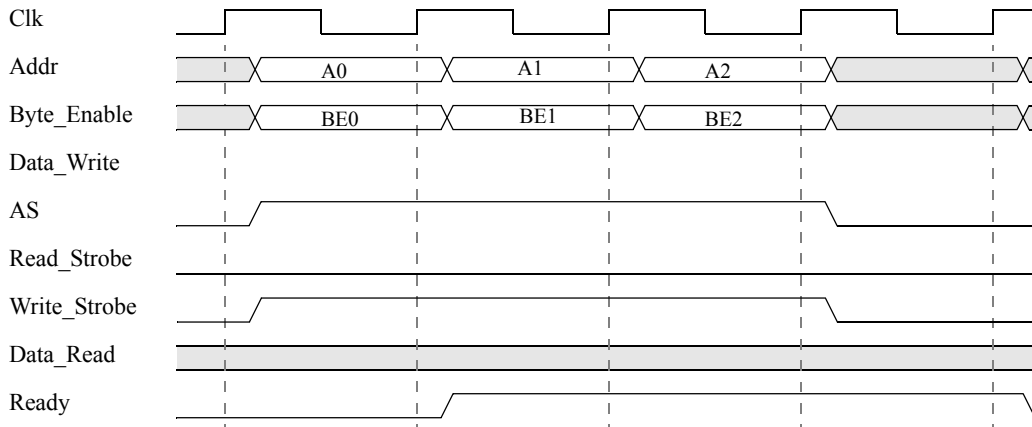


Figure 2-4: LMB Back-to-Back Write Operation

Single Cycle Back-to-Back Read Operation

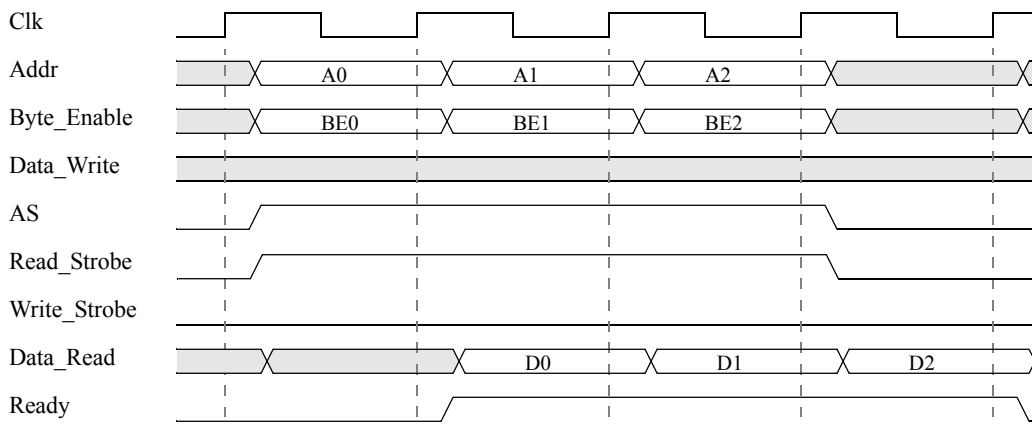


Figure 2-5: LMB Single Cycle Back-to-Back Read Operation

Back-to-Back Mixed Read/Write Operation

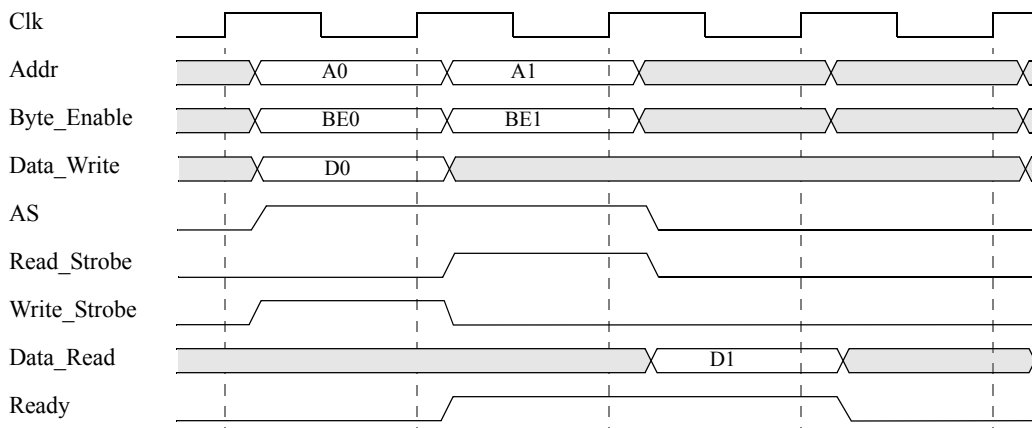


Figure 2-6: Back-to-Back Mixed Read/Write Operation

Read and Write Data Steering

The MicroBlaze data-side bus interface performs the read steering and write steering required to support the following transfers:

- byte, halfword, and word transfers to word devices
- byte and halfword transfers to halfword devices
- byte transfers to byte devices

MicroBlaze does not support transfers that are larger than the addressed device. These types of transfers require dynamic bus sizing and conversion cycles that are not supported by the MicroBlaze bus interface. Data steering for read cycles is shown in Table 2-4, and data steering for write cycles is shown in Table 2-5.

Table 2-4: Read Data Steering (Load to Register rD)

Address [30:31]	Byte_Enable [0:3]	Transfer Size	Register rD Data			
			rD[0:7]	rD[8:15]	rD[16:23]	rD[24:31]
11	0001	byte				Byte3
10	0010	byte				Byte2
01	0100	byte				Byte1
00	1000	byte				Byte0
10	0011	halfword			Byte2	Byte3
00	1100	halfword			Byte0	Byte1
00	1111	word	Byte0	Byte1	Byte2	Byte3

Table 2-5: Write Data Steering (Store from Register rD)

Address [30:31]	Byte_Enable [0:3]	Transfer Size	Write Data Bus Bytes			
			Byte0	Byte1	Byte2	Byte3
11	0001	byte				rD[24:31]
10	0010	byte			rD[24:31]	
01	0100	byte		rD[24:31]		
00	1000	byte	rD[24:31]			
10	0011	halfword			rD[16:23]	rD[24:31]
00	1100	halfword	rD[16:23]	rD[24:31]		
00	1111	word	rD[0:7]	rD[8:15]	rD[16:23]	rD[24:31]

Note: Other OPB masters may have more restrictive requirements for byte lane placement than those allowed by MicroBlaze. OPB slave devices are typically attached “left-justified” with byte devices attached to the most-significant byte lane, and halfword devices attached to the most significant halfword lane. The MicroBlaze steering logic fully supports this attachment method.

Fast Simplex Link (FSL) Interface Description

The Fast Simplex Link bus provides a point-to-point communication channel between an output FIFO and an input FIFO. For more information on the generic FSL protocol, see DS449 [Data Sheet](#).

Master FSL Signal Interface

MicroBlaze may contain up to 16 master FSL interfaces. The master signals are depicted in [Table 2-6](#).

Table 2-6: Master FSL Signals

Signal Name	Description	VHDL Type	Direction
FSLn_M_Clk	Clock	std_logic	input
FSLn_M_Write	Write enable signal indicating that data is being written to the output FSL	std_logic	output
FSLn_M_Data	Data value written to the output FSL	std_logic_vector	output
FSLn_M_Control	Control bit value written to the output FSL	std_logic	output
FSLn_M_Full	Full Bit indicating output FSL FIFO is full when set	std_logic	input

Slave FSL Signal Interface

MicroBlaze may contain up to 16 slave FSL interfaces. The slave FSL interface signals are depicted in [Table 2-7](#).

Table 2-7: Slave FSL Signals

Signal Name	Description	VHDL Type	Direction
FSLn_S_Clk	Clock	std_logic	input
FSLn_S_Read	Read acknowledge signal indicating that data has been read from the input FSL	std_logic	output
FSLn_S_Data	Data value currently available at the top of the input FSL	std_logic_vector	input
FSLn_S_Control	Control Bit value currently available at the top of the input FSL	std_logic	input
FSLn_S_Exists	Flag indicating that data exists in the input FSL	std_logic	input

FSL Transactions

FSL BUS Write Operation

A write to the FSL bus is performed by MicroBlaze using one of the put or putd instructions. A write operation transfers the register contents to an output FSL bus. The transfer is completed in a single clock cycle for blocking mode writes to the FSL (put and cput instructions) as long as the FSL FIFO does not become full. If the FSL FIFO is full, the processor stalls until the FSL full flag is lowered. The non-blocking instructions (with prefix n), always completes in a single clock cycle even if the FSL was full. If the FSL was full, the write is inhibited and the carry bit is set in the MSR.

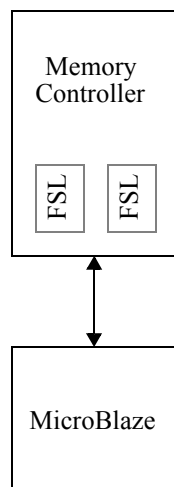
FSL BUS Read Operation

A read from the FSL bus is performed by MicroBlaze using one of the get or getd instructions. A read operations transfers the contents of an input FSL to a general purpose register. The transfer is typically completed in 2 clock cycles for blocking mode reads from the FSL as long as data exists in the FSL FIFO. If the FSL FIFO is empty, the processor stalls at this instruction until the FSL exists flag is set. In the non-blocking mode (instructions with prefix n), the transfer is completed in two clock cycles irrespective of whether or not the FSL was empty. In the case the FSL was empty, the transfer of data does not take place and the carry bit is set in the MSR.

Xilinx CacheLink (XCL) Interface Description

Xilinx CacheLink (XCL) is a high performance solution for external memory accesses. The MicroBlaze CacheLink interface is designed to connect directly to a memory controller with integrated FSL buffers, for example, the MPMC. This method has the lowest latency and minimal number of instantiations (see Figure 2-7).

Schematic



Example MHS code

```
BEGIN microblaze
  ...
  BUS_INTERFACE IXCL = myIXCL
  ...
END
BEGIN mpmc
  ...
  BUS_INTERFACE XCL0 = myIXCL
  ...
END
```

Figure 2-7: CacheLink Connection with Integrated FSL Buffers (Only Instruction Cache Used in this Example)

The interface is only available on MicroBlaze when caches are enabled. It is legal to use a CacheLink cache on the instruction side or the data side without caching the other. Memory locations outside the cacheable range are accessed over PLB, OPB or LMB. Cached memory range is accessed over PLB or OPB whenever the caches are software disabled (for example, MSR[DCE]=0 or MSR[ICE]=0).

The CacheLink cache controllers handle 4 or 8-word cache lines with critical word first. At the same time the separation from the PLB or OPB bus reduces contention for non-cached memory accesses.

CacheLink Signal Interface

The CacheLink signals on MicroBlaze are listed in [Table 2-8](#).

Table 2-8: MicroBlaze Cache Link Signals

Signal Name	Description	VHDL Type	Direction
ICACHE_FSL_IN_Clk	Clock output to I-side return read data FSL	std_logic	output
ICACHE_FSL_IN_Read	Read signal to I-side return read data FSL.	std_logic	output
ICACHE_FSL_IN_Data	Read data from I-side return read data FSL	std_logic_vector (0 to 31)	input
ICACHE_FSL_IN_Control	FSL control-bit from I-side return read data FSL. Reserved for future use	std_logic	input
ICACHE_FSL_IN_Exists	More read data exists in I-side return FSL	std_logic	input
ICACHE_FSL_OUT_Clk	Clock output to I-side read access FSL	std_logic	output
ICACHE_FSL_OUT_Write	Write new cache miss access request to I-side read access FSL	std_logic	output
ICACHE_FSL_OUT_Data	Cache miss access (=address) to I-side read access FSL	std_logic_vector (0 to 31)	output
ICACHE_FSL_OUT_Control	FSL control-bit to I-side read access FSL. Reserved for future use	std_logic	output
ICACHE_FSL_OUT_Full	FSL access buffer for I-side read accesses is full	std_logic	input
DCACHE_FSL_IN_Clk	Clock output to D-side return read data FSL	std_logic	output
DCACHE_FSL_IN_Read	Read signal to D-side return read data FSL	std_logic	output
DCACHE_FSL_IN_Data	Read data from D-side return read data FSL	std_logic_vector (0 to 31)	input

Table 2-8: MicroBlaze Cache Link Signals

Signal Name	Description	VHDL Type	Direction
DCACHE_FSL_IN_Control	FSL control bit from D-side return read data FSL	std_logic	input
DCACHE_FSL_IN_Exists	More read data exists in D-side return FSL	std_logic	input
DCACHE_FSL_OUT_Clk	Clock output to D-side read access FSL	std_logic	output
DCACHE_FSL_OUT_Write	Write new cache miss access request to D-side read access FSL	std_logic	output
DCACHE_FSL_OUT_Data	Cache miss access (read address or write address + write data + byte write enable) to D-side read access FSL	std_logic_vector (0 to 31)	output
DCACHE_FSL_OUT_Control	FSL control-bit to D-side read access FSL. Used with address bits [30 to 31] for read/write and byte enable encoding.	std_logic	output
DCACHE_FSL_OUT_Full	FSL access buffer for D-side read accesses is full	std_logic	input

CacheLink Transactions

All individual CacheLink accesses follow the FSL FIFO based transaction protocol:

- Access information is encoded over the FSL data and control signals (e.g. DCACHE_FSL_OUT_Data, DCACHE_FSL_OUT_Control, ICACHE_FSL_IN_Data, and ICACHE_FSL_IN_Control)
- Information is sent (stored) by raising the write enable signal (e.g. DCACHE_FSL_OUT_Write)
- The sender is only allowed to write if the full signal from the receiver is inactive (e.g. DCACHE_FSL_OUT_Full = 0). The full signal is not used by the instruction cache controller.
- Information is received (loaded) by raising the read signal (e.g. ICACHE_FSL_IN_Read)
- The receiver is only allowed to read as long as the sender signals that new data exists (e.g. ICACHE_FSL_IN_Exists = 1)

For details on the generic FSL protocol, please see DS449 [Data Sheet](#).

The CacheLink solution uses one incoming (slave) and one outgoing (master) FSL per cache controller. The outgoing FSL is used to send access requests, while the incoming FSL is used for receiving the requested cache lines. CacheLink also uses a specific encoding of the transaction information over the FSL data and control signals.

The cache lines used for reads in the CacheLink protocol are 4 or 8 words long. Each cache line is expected to start with the critical word first (for example, if an access to address 0x348 is a miss with

a 4 word cache line, then the returned cache line should have the following address sequence: 0x348, 0x34c, 0x340, 0x344). The cache controller forwards the first word to the execution unit as well as stores it in the cache memory. This allows execution to resume as soon as the first word is back. The cache controller then follows through by filling up the cache line with the remaining 3 or 7 words as they are received.

All write operations to the data cache are single-word write-through.

Instruction Cache Read Miss

On a read miss the cache controller performs the following sequence:

1. Write the word aligned⁽¹⁾ missed address to `ICACHE_FSL_OUT_Data`, with the control bit set low (`ICACHE_FSL_OUT_Control = 0`) to indicate a read access
 2. Wait until `ICACHE_FSL_IN_Exists` goes high to indicate that data is available
- Note:** There must be at least one clock cycle before `ICACHE_FSL_IN_Exists` goes high (for example, at least one wait state must be used).
3. Store the word from `ICACHE_FSL_IN_Data` to the cache
 4. Forward the critical word to the execution unit in order to resume execution
 5. Repeat 3 and 4 for the subsequent 3 or 7 words in the cache line

Data Cache Read Miss

On a read miss the cache controller will perform the following sequence:

1. If `DCACHE_FSL_OUT_Full = 1` then stall until it goes low
 2. Write the word aligned¹ missed address to `DCACHE_FSL_OUT_Data`, with the control bit set low (`DCACHE_FSL_OUT_Control = 0`) to indicate a read access
 3. Wait until `DCACHE_FSL_IN_Exists` goes high to indicate that data is available
- Note:** There must be at least one clock cycle before `DCACHE_FSL_IN_Exists` goes high (for example, at least one wait state must be used).
4. Store the word from `DCACHE_FSL_IN_Data` to the cache
 5. Forward the critical word to the execution unit in order to resume execution
 6. Repeat 3 and 4 for the subsequent 3 or 7 words in the cache line

Data Cache Write

Note that writes to the data cache always are write-through, and thus there is a write over the CacheLink regardless of whether there was a hit or miss in the cache. On a write, the cache controller performs the following sequence:

1. If `DCACHE_FSL_OUT_Full = 1` then stall until it goes low
2. Write the missed address to `DCACHE_FSL_OUT_Data`, with the control bit set high (`DCACHE_FSL_OUT_Control = 1`) to indicate a write access. The two least-significant bits (30:31) of the address are used to encode byte and half-word enables: 0b00=byte0, 0b01=byte1 or halfword0, 0x10=byte2, and 0x11=byte3 or halfword1. The selection of half-word or byte access is based on the control bit for the data word in step 4.
3. If `DCACHE_FSL_OUT_Full = 1` then stall until it goes low

1. Byte and halfword read misses are naturally expected to return complete words, the cache controller then provides the execution unit with the correct bytes.

4. Write the data to be stored to `DCACHE_FSL_OUT_Data`. For byte and halfword accesses the data is mirrored onto byte-lanes. Mirroring outputs the byte or halfword to be written on all four byte-lanes or on both halfword-lanes, respectively. The control bit should be low (`DCACHE_FSL_OUT_Control = 0`) for a word or halfword access, and high for a byte access. Word or halfword accesses can be distinguished by the least significant bit of the address (0=word and 1=halfword).

Debug Interface Description

The debug interface on MicroBlaze is designed to work with the Xilinx Microprocessor Debug Module (MDM) IP core. The MDM is controlled by the Xilinx Microprocessor Debugger (XMD) through the JTAG port of the FPGA. The MDM can control multiple MicroBlaze processors at the same time. The debug signals are grouped in the DEBUG bus. The debug signals on MicroBlaze are listed in [Table 2-9](#).

Table 2-9: MicroBlaze Debug Signals

Signal Name	Description	VHDL Type	Direction
<code>Dbg_Clk</code>	JTAG clock from MDM	<code>std_logic</code>	input
<code>Dbg_TDI</code>	JTAG TDI from MDM	<code>std_logic</code>	input
<code>Dbg_TDO</code>	JTAG TDO to MDM	<code>std_logic</code>	output
<code>Dbg_Reg_En</code>	Debug register enable from MDM	<code>std_logic</code>	input
<code>Dbg_Shift</code> ¹	JTAG BSCAN shift signal from MDM	<code>std_logic</code>	input
<code>Dbg_Capture</code>	JTAG BSCAN capture signal from MDM	<code>std_logic</code>	input
<code>Dbg_Update</code>	JTAG BSCAN update signal from MDM	<code>std_logic</code>	input
<code>Debug_Rst</code> ¹	Reset signal from MDM, active high. Should be held for at least 1 <code>Clk</code> clock cycle.	<code>std_logic</code>	input

1. Updated for MicroBlaze v7.00: `Dbg_Shift` added and `Debug_Rst` included in DEBUG bus

Trace Interface Description

The MicroBlaze core exports a number of internal signals for trace purposes. This signal interface is not standardized and new revisions of the processor may not be backward compatible for signal selection or functionality. It is recommended that you not design custom logic for these signals, but rather to use them via Xilinx provided analysis IP. The trace signals are grouped in the TRACE bus. The current set of trace signals were last updated for MicroBlaze v7.00 and are listed in [Table 2-10](#). The Trace exception types are listed in [Table 2-11](#). All unused Trace exception types are reserved.

Table 2-10: MicroBlaze Trace Signals

Signal Name	Description	VHDL Type	Direction
Trace_Valid_Instr	Valid instruction on trace port.	std_logic	output
Trace_Instruction ¹	Instruction code	std_logic_vector (0 to 31)	output
Trace_PC ¹	Program counter	std_logic_vector (0 to 31)	output
Trace_Reg_Write ¹	Instruction writes to the register file	std_logic	output
Trace_Reg_Addr ¹	Destination register address	std_logic_vector (0 to 4)	output
Trace_MSR_Reg ¹	Machine status register	std_logic_vector (0 to 14) ²	output
Trace_PID_Reg ^{1,2}	Process identifier register	std_logic_vector (0 to 7)	output
Trace_New_Reg_Value ¹	Destination register update value	std_logic_vector (0 to 31)	output
Trace_Exception_Taken ¹	Instruction result in taken exception	std_logic	output
Trace_Exception_Kind ^{1,3}	Exception type. The description for the exception type is documented below.	std_logic_vector (0 to 4) ²	output
Trace_Jump_Taken ¹	Branch instruction evaluated true, i.e taken	std_logic	output
Trace_Delay_Slot ¹	Instruction is in delay slot of a taken branch	std_logic	output
Trace_Data_Access ¹	Valid D-side memory access	std_logic	output
Trace_Data_Address ¹	Address for D-side memory access	std_logic_vector (0 to 31)	output
Trace_Data_Write_Value ¹	Value for D-side memory write access	std_logic_vector (0 to 31)	output
Trace_Data_Byte_Enable ¹	Byte enables for D-side memory access	std_logic_vector (0 to 3)	output
Trace_Data_Read ¹	D-side memory access is a read	std_logic	output
Trace_Data_Write ¹	D-side memory access is a write	std_logic	output
Trace_DCache_Req	Data memory address is within D-Cache range	std_logic	output

Table 2-10: MicroBlaze Trace Signals

Signal Name	Description	VHDL Type	Direction
Trace_DCache_Hit	Data memory address is present in D-Cache	std_logic	output
Trace_ICache_Req	Instruction memory address is in I-Cache range	std_logic	output
Trace_ICache_Hit	Instruction memory address is present in I-Cache	std_logic	output
Trace_OF_PipeRun	Pipeline advance for Decode stage	std_logic	output
Trace_EX_PipeRun ⁴	Pipeline advance for Execution stage	std_logic	output
Trace_MEM_PipeRun ³	Pipeline advance for Memory stage	std_logic	output

1. Valid only when Trace_Valid_Instr = 1
2. Updated for MicroBlaze v7.00: 4 bits added to Trace_MSR_Reg, Trace_PID_Reg added, and 1 bit added to Trace_Exception Kind
3. Valid only when Trace_Exception_Taken = 1
4. Not used with area optimization feature

Table 2-11: Type of Trace Exception

Trace_Exception_Kind [0:4]	Description
00000	Fast Simplex Link exception ¹
00001	Unaligned exception
00010	Illegal Opcode exception
00011	Instruction Bus exception
00100	Data Bus exception
00101	Div by Zero exception
00110	FPU exception
00111	Privileged instruction exception ¹
01010	Interrupt
01011	External non maskable break
01100	External maskable break
10000	Data storage exception ¹
10001	Instruction storage exception ¹
10010	Data TLB miss exception ¹
10011	Instruction TLB miss exception ¹

1. Added for MicroBlaze v7.00

MicroBlaze Core Configurability

The MicroBlaze core has been developed to support a high degree of user configurability. This allows tailoring of the processor to meet specific cost/performance requirements.

Configuration is done via parameters that typically enable, size, or select certain processor features. For example, the instruction cache is enabled by setting the `C_USE_ICACHE` parameter. The size of the instruction cache, and the cacheable memory range, are all configurable using:

`C_CACHE_BYTE_SIZE`, `C_ICACHE_BASEADDR`, and `C_ICACHE_HIGHADDR` respectively.

Parameters valid for MicroBlaze v7.00 are listed in [Table 2-12](#). Not all of these are recognized by older versions of MicroBlaze; however, the configurability is fully backward compatibility.

Note: Shaded rows indicate that the parameter has a fixed value and *cannot* be modified.

Table 2-12: MPD Parameters

Parameter Name	Feature/Description	Allowable Values	Default Value	EDK Tool Assigned	VHDL Type
<code>C_FAMILY</code>	Target Family	qrvirtex2 qvirtex2 spartan3 spartan3a spartan3adsp spartan3an spartan3e virtex2 virtex2p virtex4 virtex5	virtex2	yes	string
<code>C_DATA_SIZE</code>	Data Size	32	32	NA	integer
<code>C_DYNAMIC_BUS_SIZING</code>	Legacy	1	1	NA	integer
<code>C_SCO</code>	Xilinx internal	0	0	NA	integer
<code>C_AREA_OPTIMIZED</code>	Select speed optimization	0, 1	0		integer
<code>C_INTERCONNECT</code>	Select PLB interconnect	0, 1	1		integer
<code>C_PVR</code>	Processor version register mode selection	0, 1, 2	0		integer
<code>C_PVR_USER1</code>	Processor version register USER1 constant	0x00-0xff	0x00		std_logic_vector (0 to 7)
<code>C_PVR_USER2</code>	Processor version register USER2 constant	0x00000000-0xffffffff	0x00000000		std_logic_vector (0 to 31)
<code>C_RESET_MSR</code>	Reset value for MSR register	0x00, 0x20, 0x80, 0xa0	0x00		std_logic_vector
<code>C_INSTANCE</code>	Instance Name	Any instance name	microblaze	yes	string
<code>C_D_PLB</code>	Data side PLB interface	0, 1	1	yes	integer

Table 2-12: MPD Parameters (Continued)

Parameter Name	Feature/Description	Allowable Values	Default Value	EDK Tool Assigned	VHDL Type
C_D_OPB	Data side OPB interface	0, 1	1	yes	integer
C_D_LMB	Data side LMB interface	0, 1	1	yes	integer
C_I_PLB	Instruction side PLB interface	0, 1	1	yes	integer
C_I_OPB	Instruction side OPB interface	0, 1	1	yes	integer
C_I_LMB	Instruction side LMB interface	0, 1	1	yes	integer
C_USE_BARREL	Include barrel shifter	0, 1	0		integer
C_USE_DIV	Include hardware divider	0, 1	0		integer
C_USE_HW_MUL	Include hardware multiplier (Virtex2 and later)	0, 1, 2	1		integer
C_USE_FPU	Include hardware floating point unit (Virtex2 and later)	0, 1, 2	0		integer
C_USE_MSR_INSTR	Enable use of instructions: MSRSET and MSRCLR	0, 1	0		integer
C_USE_PCOMP_INSTR	Enable use of instructions: PCOMPBF, PCMPPEQ, and PCMPNE	0, 1	0		integer
C_UNALIGNED_EXCEPTION	Enable exception handling for unaligned data accesses	0, 1	0		integer
C_ILL_OPCODE_EXCEPTION	Enable exception handling for illegal op-code	0, 1	0		integer
C_IPLB_BUS_EXCEPTION	Enable exception handling for IPLB bus error	0, 1	0		integer
C_DPLB_BUS_EXCEPTION	Enable exception handling for DPLB bus error	0, 1	0		integer
C_IOPB_BUS_EXCEPTION	Enable exception handling for IOPB bus error	0, 1	0		integer
C_DOPB_BUS_EXCEPTION	Enable exception handling for DOPB bus error	0, 1	0		integer
C_DIV_ZERO_EXCEPTION	Enable exception handling for division by zero	0, 1	0		integer

Table 2-12: MPD Parameters (Continued)

Parameter Name	Feature/Description	Allowable Values	Default Value	EDK Tool Assigned	VHDL Type
C_FPU_EXCEPTION	Enable exception handling for hardware floating point unit exceptions	0, 1	0		integer
C_OPCODE_0x0_ILLEGAL	Detect opcode 0x0 as an illegal instruction	0,1	0		integer
C_FSL_EXCEPTION	Enable exception handling for Fast Simplex Link	0,1	0		integer
C_DEBUG_ENABLED	MDM Debug interface	0,1	0		integer
C_NUMBER_OF_PC_BRK	Number of hardware breakpoints	0-8	1		integer
C_NUMBER_OF_RD_ADDR_BRK	Number of read address watchpoints	0-4	0		integer
C_NUMBER_OF_WR_ADDR_BRK	Number of write address watchpoints	0-4	0		integer
C_INTERRUPT_IS_EDGE	Level/Edge Interrupt	0, 1	0		integer
C_EDGE_IS_POSITIVE	Negative/Positive Edge Interrupt	0, 1	1		integer
C_FSL_LINKS ¹	Number of FSL interfaces	0-16	0	yes	integer
C_FSL_DATA_SIZE	FSL data bus size	32	32	NA	integer
C_USE_EXTENDED_FSL_INSTR	Enable use of extended FSL instructions	0, 1	0		integer
C_ICACHE_BASEADDR	Instruction cache base address	0x00000000 - 0xFFFFFFFF	0x00000000		std_logic_vector
C_ICACHE_HIGHADDR	Instruction cache high address	0x00000000 - 0xFFFFFFFF	0x3FFF FFFF		std_logic_vector
C_USE_ICACHE	Instruction cache	0, 1	0		integer
C_ALLOW_ICACHE_WR	Instruction cache write enable	0, 1	1		integer
C_ICACHE_LINELEN	Instruction cache line length	4, 8	4		integer
C_ADDR_TAG_BITS	Instruction cache address tags	0-25	17	yes	integer

Table 2-12: MPD Parameters (Continued)

Parameter Name	Feature/Description	Allowable Values	Default Value	EDK Tool Assigned	VHDL Type
C_CACHE_BYTE_SIZE	Instruction cache size	64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768, 65536 ²	8192		integer
C_ICACHE_USE_FSL	Cache over CacheLink instead of OPB for instructions	1	1		integer
C_DCACHE_BASEADDR	Data cache base address	0x00000000 - 0xFFFFFFFF	0x00000000		std_logic_vector
C_DCACHE_HIGHADDR	Data cache high address	0x00000000 - 0xFFFFFFFF	0x3FFF FFFF		std_logic_vector
C_USE_DCACHE	Data cache	0,1	0		integer
C_ALLOW_DCACHE_WR	Data cache write enable	0,1	1		integer
C_DCACHE_LINELEN	Data cache line length	4, 8	4		integer
C_DCACHE_ADDR_TAG	Data cache address tags	0-25	17	yes	integer
C_DCACHE_BYTE_SIZE	Data cache size	64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768, 65536 ²	8192		integer
C_DCACHE_USE_FSL	Cache over CacheLink instead of OPB for data	1	1		integer
C_DPLB_DWIDTH	Data side PLB data width	32	32		integer
C_DPLB_NATIVE_DWIDTH	Data side PLB native data width	32	32		integer
C_DPLB_BURST_EN	Data side PLB burst enable	0	0		integer
C_DPLB_P2P	Data side PLB Point-to-point	0, 1	0		integer
C_IPLB_DWIDTH	Instruction side PLB data width	32	32		integer
C_IPLB_NATIVE_DWIDTH	Instruction side PLB native data width	32	32		integer
C_IPLB_BURST_EN	Instruction side PLB burst enable	0	0		integer

Table 2-12: MPD Parameters (Continued)

Parameter Name	Feature/Description	Allowable Values	Default Value	EDK Tool Assigned	VHDL Type
C_IPLB_P2P	Instruction side PLB Point-to-point	0, 1	0		integer
C_USE_MMU	Memory Management: 0 = None 1 = Usermode 2 = Protection 3 = Virtual	0, 1, 2, 3	0		integer
C_MMU_DTLB_SIZE	Data shadow Translation Look-Aside Buffer size	1, 2, 4, 8	8		integer
C_MMU_ITLB_SIZE	Instruction shadow Translation Look-Aside Buffer size	1, 2, 4, 8	4		integer
C_MMU_TLB_ACCESS	Access to memory management special registers: 0 = Minimal 1 = Read 2 = Write 3 = Full	0, 1, 2, 3	3		integer
C_MMU_ZONES	Number of memory protection zones	0-16	16		integer

1. The number of FSL Links is assigned by the tool itself if you are using the co-processor wizard. If you add the IP manually, you must update the parameter manually.
2. Not all sizes are permitted in all architectures. The cache uses between 0 and 32 RAMB primitives (0 if cache size is less than 2048).

MicroBlaze Application Binary Interface

This chapter describes MicroBlaze™ Application Binary Interface (ABI), which is important for developing software in assembly language for the soft processor. The MicroBlaze GNU compiler follows the conventions described in this document. Any code written by assembly programmers should also follow the same conventions to be compatible with the compiler generated code. Interrupt and Exception handling is also explained briefly.

This chapter contains the following sections:

- “Data Types”
- “Register Usage Conventions”
- “Stack Convention”
- “Memory Model”
- “Interrupt and Exception Handling”

Data Types

The data types used by MicroBlaze assembly programs are shown in [Table 3-1](#). Data types such as data8, data16, and data32 are used in place of the usual byte, half-word, and word.register

Table 3-1: Data Types in MicroBlaze Assembly Programs

MicroBlaze data types (for assembly programs)	Corresponding ANSI C data types	Size (bytes)
data8	char	1
data16	short	2
data32	int	4
data32	long int	4
data32	float	4
data32	enum	4
data16/data32	pointer ^a	2/4

a. Pointers to small data areas, which can be accessed by global pointers are data16.

Register Usage Conventions

The register usage convention for MicroBlaze is given in [Table 3-2](#).

Table 3-2: Register Usage Conventions

Register	Type	Enforcement	Purpose
R0	Dedicated	HW	Value 0
R1	Dedicated	SW	Stack Pointer
R2	Dedicated	SW	Read-only small data area anchor
R3-R4	Volatile	SW	Return Values/Temporaries
R5-R10	Volatile	SW	Passing parameters/Temporaries
R11-R12	Volatile	SW	Temporaries
R13	Dedicated	SW	Read-write small data area anchor
R14	Dedicated	HW	Return address for Interrupt
R15	Dedicated	SW	Return address for Sub-routine
R16	Dedicated	HW	Return address for Trap (Debugger)
R17	Dedicated	HW, if configured to support HW exceptions, else SW	Return address for Exceptions
R18	Dedicated	SW	Reserved for Assembler
R19-R31	Non-volatile	SW	Must be saved across function calls. Callee-save
RPC	Special	HW	Program counter
RMSR	Special	HW	Machine Status Register
REAR	Special	HW	Exception Address Register
RESR	Special	HW	Exception Status Register
RFSR	Special	HW	Floating Point Status Register
RBTR	Special	HW	Branch Target Register
REDR	Special	HW	Exception Data Register
RPID	Special	HW	Process Identifier Register
RZPR	Special	HW	Zone Protection Register
RTLBLO	Special	HW	Translation Look-Aside Buffer Low Register
RTLBHI	Special	HW	Translation Look-Aside Buffer High Register
RTLBX	Special	HW	Translation Look-Aside Buffer Index Register

Table 3-2: Register Usage Conventions

Register	Type	Enforcement	Purpose
RTLBSX	Special	HW	Translation Look-Aside Buffer Search Index
RPVR0- RPVR11	Special	HW	Processor Version Register 0 through 11

The architecture for MicroBlaze defines 32 general purpose registers (GPRs). These registers are classified as volatile, non-volatile, and dedicated.

- The volatile registers (also known as caller-save) are used as temporaries and do not retain values across the function calls. Registers R3 through R12 are volatile, of which R3 and R4 are used for returning values to the caller function, if any. Registers R5 through R10 are used for passing parameters between subroutines.
- Registers R19 through R31 retain their contents across function calls and are hence termed as non-volatile registers (a.k.a callee-save). The callee function is expected to save those non-volatile registers, which are being used. These are typically saved to the stack during the prologue and then reloaded during the epilogue.
- Certain registers are used as dedicated registers and programmers are not expected to use them for any other purpose.
 - ◆ Registers R14 through R17 are used for storing the return address from interrupts, subroutines, traps, and exceptions in that order. Subroutines are called using the branch and link instruction, which saves the current Program Counter (PC) onto register R15.
 - ◆ Small data area pointers are used for accessing certain memory locations with 16-bit immediate value. These areas are discussed in the memory model section of this document. The read only small data area (SDA) anchor R2 (Read-Only) is used to access the constants such as literals. The other SDA anchor R13 (Read-Write) is used for accessing the values in the small data read-write section.
 - ◆ Register R1 stores the value of the stack pointer and is updated on entry and exit from functions.
 - ◆ Register R18 is used as a temporary register for assembler operations.
- MicroBlaze includes special purpose registers such as: program counter (rpc), machine status register (rmsr), exception status register (resr), exception address register (rear), floating point status register (rfsr), branch target register (rbtr), exception data register (redr), memory management registers (rpid, rzpr, rtlblo, rtlbhi, rtlbx, rtlbsx), and processor version registers (rpvr0-rpvr11). These registers are not mapped directly to the register file and hence the usage of these registers is different from the general purpose registers. The value of a special purpose registers can be transferred to or from a general purpose register by using **mts** and **mfs** instructions respectively.

Stack Convention

The stack conventions used by MicroBlaze are detailed in [Table 3-3](#).

The shaded area in [Table 3-3](#) denotes a part of the stack frame for a caller function, while the unshaded area indicates the callee frame function. The ABI conventions of the stack frame define the protocol for passing parameters, preserving non-volatile register values, and allocating space for the local variables in a function.

Functions that contain calls to other subroutines are called as non-leaf functions. These non-leaf functions have to create a new stack frame area for its own use. When the program starts executing,

the stack pointer has the maximum value. As functions are called, the stack pointer is decremented by the number of words required by every function for its stack frame. The stack pointer of a caller function always has a higher value as compared to the callee function.

Table 3-3: Stack Convention

High Address	
	Function Parameters for called sub-routine (Arg n .. Arg1) (Optional: Maximum number of arguments required for any called procedure from the current procedure).
Old Stack Pointer	Link Register (R15)
	Callee Saved Register (R31....R19) (Optional: Only those registers which are used by the current procedure are saved)
	Local Variables for Current Procedure (Optional: Present only if Locals defined in the procedure)
	Functional Parameters (Arg n .. Arg 1) (Optional: Maximum number of arguments required for any called procedure from the current procedure)
New Stack Pointer	Link Register
Low Address	

Consider an example where Func1 calls Func2, which in turn calls Func3. The stack representation at different instances is depicted in Figure 3-1. After the call from Func 1 to Func 2, the value of the stack pointer (SP) is decremented. This value of SP is again decremented to accommodate the stack frame for Func3. On return from Func 3 the value of the stack pointer is increased to its original value in the function, Func 2.

Details of how the stack is maintained are shown in Figure 3-1.

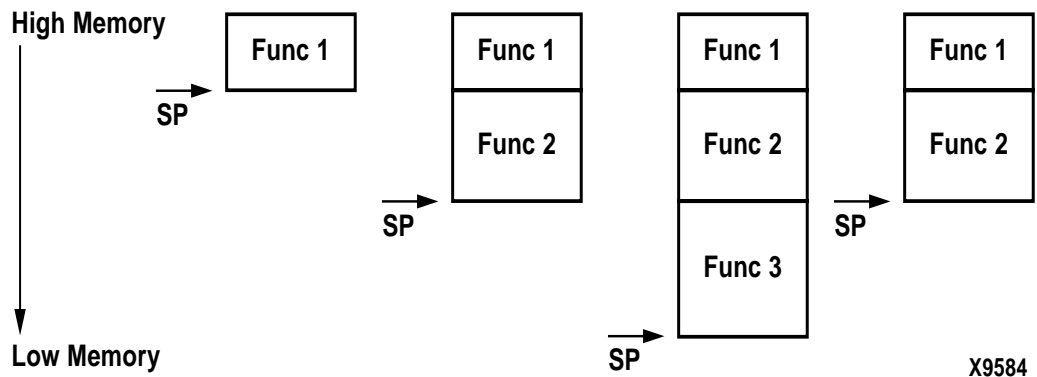


Figure 3-1: Stack Frame

X9584

Calling Convention

The caller function passes parameters to the callee function using either the registers (R5 through R10) or on its own stack frame. The callee uses the stack area of the caller to store the parameters passed to the callee.

Refer to [Figure 3-1](#). The parameters for Func 2 are stored either in the registers R5 through R10 or on the stack frame allocated for Func 1.

Memory Model

The memory model for MicroBlaze classifies the data into four different parts: Small Data Area, Data Area, Common Un-Initialized Area, and Literals or Constants.

Small Data Area

Global initialized variables which are small in size are stored in this area. The threshold for deciding the size of the variable to be stored in the small data area is set to 8 bytes in the MicroBlaze C compiler (mb-gcc), but this can be changed by giving a command line option to the compiler. Details about this option are discussed in the *GNU Compiler Tools* chapter. 64 kilobytes of memory is allocated for the small data areas. The small data area is accessed using the read-write small data area anchor (R13) and a 16-bit offset. Allocating small variables to this area reduces the requirement of adding **IMM** instructions to the code for accessing global variables. Any variable in the small data area can also be accessed using an absolute address.

Data Area

Comparatively large initialized variables are allocated to the data area, which can either be accessed using the read-write SDA anchor R13 or using the absolute address, depending on the command line option given to the compiler.

Common Un-Initialized Area

Un-initialized global variables are allocated in the common area and can be accessed either using the absolute address or using the read-write small data area anchor R13.

Literals or Constants

Constants are placed into the read-only small data area and are accessed using the read-only small data area anchor R2.

The compiler generates appropriate global pointers to act as base pointers. The actual values of the SDA anchors are decided by the linker, in the final linking stages. For more information on the various sections of the memory please refer to the *Address Management* chapter. The compiler generates appropriate sections, depending on the command line options. Please refer to the *GNU Compiler Tools* chapter for more information about these options.

Interrupt and Exception Handling

MicroBlaze assumes certain address locations for handling interrupts and exceptions as indicated in Table 3-4. At these locations, code is written to jump to the appropriate handlers.

Table 3-4: Interrupt and Exception Handling

On	Hardware jumps to	Software Labels
Start / Reset	0x0	_start
User exception	0x8	_exception_handler
Interrupt	0x10	_interrupt_handler
Break (HW/SW)	0x18	-
Hardware exception	0x20	_hw_exception_handler
Reserved by Xilinx for future use	0x28 - 0x4F	-

The code expected at these locations is as shown below. For programs compiled without the `-x1-mode-xmdstub` compiler option, the `crt0.o` initialization file is passed by the `mb-gcc` compiler to the `mb-ld` linker for linking. This file sets the appropriate addresses of the exception handlers.

For programs compiled with the `-x1-mode-xmdstub` compiler option, the `crt1.o` initialization file is linked to the output program. This program has to be run with the `xmdstub` already loaded in the memory at address location 0x0. Hence at run-time, the initialization code in `crt1.o` writes the appropriate instructions to location 0x8 through 0x14 depending on the address of the exception and interrupt handlers.

The following is code for passing control to Exception and Interrupt handlers:

```

0x00:  bri    _start1
0x04:  nop
0x08:  imm    high bits of address (user exception handler)
0x0c:  bri    _exception_handler
0x10:  imm    high bits of address (interrupt handler)
0x14:  bri    _interrupt_handler
0x20:  imm    high bits of address (HW exception handler)
0x24:  bri    _hw_exception_handler

```

MicroBlaze allows exception and interrupt handler routines to be located at any address location addressable using 32 bits. The user exception handler code starts with the label `_exception_handler`, the hardware exception handler starts with `_hw_exception_handler`, while the interrupt handler code starts with the label `_interrupt_handler`.

In the current MicroBlaze system, there are dummy routines for interrupt and exception handling, which you can change. In order to override these routines and link your interrupt and exception handlers, you must define the interrupt handler code with an attribute `interrupt_handler`. For more details about the use and syntax of the interrupt handler attribute, please refer to the *GNU Compiler Tools* chapter in the *Embedded System Tools Reference Guide*.

When software breakpoints are used in the Xilinx Microprocessor Debug (XMD) tool, the Break (HW/SW) address location is reserved for handling the software breakpoint.

MicroBlaze Instruction Set Architecture

This chapter provides a detailed guide to the Instruction Set Architecture of MicroBlaze™ and contains the following sections:

- “Notation”
- “Formats”
- “Instructions”

Notation

The symbols used throughout this chapter are defined in [Table 4-1](#).

Table 4-1: Symbol Notation

Symbol	Meaning
+	Add
-	Subtract
×	Multiply
^	Bitwise logical AND
∨	Bitwise logical OR
⊕	Bitwise logical XOR
x	Bitwise logical complement of x
←	Assignment
>>	Right shift
<<	Left shift
rx	Register x
$x[i]$	Bit i in register x
$x[i:j]$	Bits i through j in register x
=	Equal comparison
≠	Not equal comparison
>	Greater than comparison
>=	Greater than or equal comparison

Table 4-1: Symbol Notation (Continued)

Symbol	Meaning
<	Less than comparison
<=	Less than or equal comparison
sext(<i>x</i>)	Sign-extend <i>x</i>
Mem(<i>x</i>)	Memory location at address <i>x</i>
FSL <i>x</i>	FSL interface <i>x</i>
LSW(<i>x</i>)	Least Significant Word of <i>x</i>
isDnz(<i>x</i>)	Floating point: true if <i>x</i> is denormalized
isInfinite(<i>x</i>)	Floating point: true if <i>x</i> is $+\infty$ or $-\infty$
isPosInfinite(<i>x</i>)	Floating point: true if <i>x</i> is $+\infty$
isNegInfinite(<i>x</i>)	Floating point: true if <i>x</i> is $-\infty$
isNaN(<i>x</i>)	Floating point: true if <i>x</i> is a quiet or signalling NaN
isZero(<i>x</i>)	Floating point: true if <i>x</i> is $+0$ or -0
isQuietNaN(<i>x</i>)	Floating point: true if <i>x</i> is a quiet NaN
isSigNaN(<i>x</i>)	Floating point: true if <i>x</i> is a signaling NaN
signZero(<i>x</i>)	Floating point: return $+0$ for $x > 0$, and -0 if $x < 0$
signInfinite(<i>x</i>)	Floating point: return $+\infty$ for $x > 0$, and $-\infty$ if $x < 0$

Formats

MicroBlaze uses two instruction formats: Type A and Type B.

Type A

Type A is used for register-register instructions. It contains the opcode, one destination and two source registers.

Opcode	Destination Reg	Source Reg A	Source Reg B	0	0	0	0	0	0	0	0	0	0	0
0	6	1	1	2										3
		1	6	1										1

Type B

Type B is used for register-immediate instructions. It contains the opcode, one destination and one source registers, and a source 16-bit immediate value.

Opcode	Destination Reg	Source Reg A	Immediate Value
0	6	1	1
		1	6
			3
			1

Instructions

This section provides descriptions of MicroBlaze instructions. Instructions are listed in alphabetical order. For each instruction Xilinx® provides the mnemonic, encoding, a description, pseudocode of its semantics, and a list of registers that it modifies.

add

Arithmetic Add

add	rD, rA, rB	Add
addc	rD, rA, rB	Add with Carry
addk	rD, rA, rB	Add and Keep Carry
addkc	rD, rA, rB	Add with Carry and Keep Carry

0 0 0 K C 0	rD	rA	rB	0 0 0 0 0 0 0 0 0 0 0 0
0	6	1	1	2
		1	6	1
				3
				1

Description

The sum of the contents of registers rA and rB, is placed into register rD.

Bit 3 of the instruction (labeled as K in the figure) is set to one for the mnemonic addk. Bit 4 of the instruction (labeled as C in the figure) is set to one for the mnemonic addc. Both bits are set to one for the mnemonic addkc.

When an add instruction has bit 3 set (addk, addkc), the carry flag will Keep its previous value regardless of the outcome of the execution of the instruction. If bit 3 is cleared (add, addc), then the carry flag will be affected by the execution of the instruction.

When bit 4 of the instruction is set to one (addc, addkc), the content of the carry flag (MSR[C]) affects the execution of the instruction. When bit 4 is cleared (add, addk), the content of the carry flag does not affect the execution of the instruction (providing a normal addition).

Pseudocode

```

if C = 0 then
    (rD) ← (rA) + (rB)
else
    (rD) ← (rA) + (rB) + MSR[C]
if K = 0 then
    MSR[C] ← CarryOut
    
```

Registers Altered

- rD
- MSR[C]

Latency

1 cycle

Note

The C bit in the instruction opcode is not the same as the carry bit in the MSR.

The “add r0, r0, r0” (= 0x00000000) instruction is never used by the compiler and usually indicates uninitialized memory. If you are using illegal instruction exceptions you can trap these instructions by setting the MicroBlaze parameter C_OPCODE_0x0_ILLEGAL=1.

addi

Arithmetic Add Immediate

addi	rD, rA, IMM	Add Immediate
addic	rD, rA, IMM	Add Immediate with Carry
addik	rD, rA, IMM	Add Immediate and Keep Carry
addikc	rD, rA, IMM	Add Immediate with Carry and Keep Carry

0 0 1 K C 0	rD	rA	IMM
0	6	1	1
		1	6
			3
			1

Description

The sum of the contents of registers rA and the value in the IMM field, sign-extended to 32 bits, is placed into register rD. Bit 3 of the instruction (labeled as K in the figure) is set to one for the mnemonic addik. Bit 4 of the instruction (labeled as C in the figure) is set to one for the mnemonic addic. Both bits are set to one for the mnemonic addikc.

When an addi instruction has bit 3 set (addik, addikc), the carry flag will keep its previous value regardless of the outcome of the execution of the instruction. If bit 3 is cleared (addi, addic), then the carry flag will be affected by the execution of the instruction.

When bit 4 of the instruction is set to one (addic, addikc), the content of the carry flag (MSR[C]) affects the execution of the instruction. When bit 4 is cleared (addi, addik), the content of the carry flag does not affect the execution of the instruction (providing a normal addition).

Pseudocode

```

if C = 0 then
  (rD) ← (rA) + sext(IMM)
else
  (rD) ← (rA) + sext(IMM) + MSR[C]
if K = 0 then
  MSR[C] ← CarryOut

```

Registers Altered

- rD
- MSR[C]

Latency

1 cycle

Notes

The C bit in the instruction opcode is not the same as the carry bit in the MSR.

By default, Type B Instructions take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” [page 147](#) for details on using 32-bit immediate values.

and

Logical AND

and rD, rA, rB

1	0	0	0	0	1	rD	rA	rB	0	0	0	0	0	0	0	0	0	0	0
0						6	1	1	2										3
							1	6	1										1

Description

The contents of register rA are ANDed with the contents of register rB; the result is placed into register rD.

Pseudocode

$$(rD) \leftarrow (rA) \wedge (rB)$$

Registers Altered

- rD

Latency

1 cycle

andi

Logical AND with Immediate

andi rD, rA, IMM

1	0	1	0	0	1	rD	rA	IMM
0					6	1	1	3
						1	6	1

Description

The contents of register rA are ANDed with the value of the IMM field, sign-extended to 32 bits; the result is placed into register rD.

Pseudocode

$$(rD) \leftarrow (rA) \wedge \text{sext}(IMM)$$

Registers Altered

- rD

Latency

1 cycle

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

andn

Logical AND NOT

andn rD, rA, rB

1	0	0	0	1	1	rD	rA	rB	0	0	0	0	0	0	0	0	0	0	0	
0						6	1	1	2											3
							1	6	1											1

Description

The contents of register rA are ANDed with the logical complement of the contents of register rB; the result is placed into register rD.

Pseudocode

$$(rD) \leftarrow (rA) \wedge (\overline{rB})$$

Registers Altered

- rD

Latency

1 cycle

andni

Logical AND NOT with Immediate

andni rD, rA, IMM

1	0	1	0	1	1	rD	rA	IMM
0					6	1	1	3
						1	6	1

Description

The IMM field is sign-extended to 32 bits. The contents of register rA are ANDed with the logical complement of the extended IMM field; the result is placed into register rD.

Pseudocode

$$(rD) \leftarrow (rA) \wedge (\overline{\text{sext}(IMM)})$$

Registers Altered

- rD

Latency

1 cycle

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

beq

Branch if Equal

beq	rA, rB	Branch if Equal
beqd	rA, rB	Branch if Equal with Delay

1	0	0	1	1	1	D	0	0	0	0	rA	rB	0	0	0	0	0	0	0	0	0	0	
0						6						1		1		2						3	
												1		6		1						1	

Description

Branch if rA is equal to 0, to the instruction located in the offset value of rB. The target of the branch will be the instruction at address PC + rB.

The mnemonic beqd will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA = 0 then
    PC ← PC + rB
else
    PC ← PC + 4
if D = 1 then
    allow following instruction to complete execution
    
```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

beqi

Branch Immediate if Equal

beqi	rA, IMM	Branch Immediate if Equal
beqid	rA, IMM	Branch Immediate if Equal with Delay

1	0	1	1	1	1	D	0	0	0	0	rA	IMM	
0						6					1	1	3
											1	6	1

Description

Branch if rA is equal to 0, to the instruction located in the offset value of IMM. The target of the branch will be the instruction at address PC + IMM.

The mnemonic beqid will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA = 0 then
    PC ← PC + sext (IMM)
else
    PC ← PC + 4
if D = 1 then
    allow following instruction to complete execution

```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

bge

Branch if Greater or Equal

bge	rA, rB	Branch if Greater or Equal
bged	rA, rB	Branch if Greater or Equal with Delay

1	0	0	1	1	1	D	0	1	0	1	rA	rB	0	0	0	0	0	0	0	0	0	0
0						6					1		1		2						3	
											1		6		1						1	

Description

Branch if rA is greater or equal to 0, to the instruction located in the offset value of rB. The target of the branch will be the instruction at address PC + rB.

The mnemonic bged will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA >= 0 then
    PC ← PC + rB
else
    PC ← PC + 4
if D = 1 then
    allow following instruction to complete execution
    
```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

bgei

Branch Immediate if Greater or Equal

bgei	rA, IMM	Branch Immediate if Greater or Equal
bgeid	rA, IMM	Branch Immediate if Greater or Equal with Delay

1 0 1 1 1 1	D 0 1 0 1	rA	IMM
0	6	1	3
		1	1

Description

Branch if rA is greater or equal to 0, to the instruction located in the offset value of IMM. The target of the branch will be the instruction at address PC + IMM.

The mnemonic bgeid will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA >= 0 then
    PC ← PC + sext(IMM)
else
    PC ← PC + 4
if D = 1 then
    allow following instruction to complete execution

```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “[imm,](#)” page 147 for details on using 32-bit immediate values.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

bgt

Branch if Greater Than

bgt	rA, rB	Branch if Greater Than
bgtD	rA, rB	Branch if Greater Than with Delay

1	0	0	1	1	1	D	0	1	0	0	rA	rB	0	0	0	0	0	0	0	0	0	0				
0						6					1		1		2										3	
											1		6		1										1	

Description

Branch if rA is greater than 0, to the instruction located in the offset value of rB. The target of the branch will be the instruction at address PC + rB.

The mnemonic bgtD will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA > 0 then
    PC ← PC + rB
else
    PC ← PC + 4
if D = 1 then
    allow following instruction to complete execution
    
```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

bgti

Branch Immediate if Greater Than

bgti	rA, IMM	Branch Immediate if Greater Than
bgtid	rA, IMM	Branch Immediate if Greater Than with Delay

1	0	1	1	1	1	D	0	1	0	0	rA	IMM
0						6					1	1
											1	6
												3
												1

Description

Branch if rA is greater than 0, to the instruction located in the offset value of IMM. The target of the branch will be the instruction at address PC + IMM.

The mnemonic bgtid will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA > 0 then
  PC ← PC + sext (IMM)
else
  PC ← PC + 4
if D = 1 then
  allow following instruction to complete execution

```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “[imm,](#)” [page 147](#) for details on using 32-bit immediate values.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

ble

Branch if Less or Equal

ble	rA, rB	Branch if Less or Equal
bled	rA, rB	Branch if Less or Equal with Delay

1	0	0	1	1	1	D	0	0	1	1	rA	rB	0	0	0	0	0	0	0	0	0	0	
0						6						1		1		2						3	
												1		6		1						1	

Description

Branch if rA is less or equal to 0, to the instruction located in the offset value of rB. The target of the branch will be the instruction at address PC + rB.

The mnemonic bled will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA <= 0 then
    PC ← PC + rB
else
    PC ← PC + 4
if D = 1 then
    allow following instruction to complete execution
    
```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

blei

Branch Immediate if Less or Equal

blei	rA, IMM	Branch Immediate if Less or Equal
bleid	rA, IMM	Branch Immediate if Less or Equal with Delay

1	0	1	1	1	1	D	0	0	1	1	rA	IMM	
0						6					1	1	3
											1	6	1

Description

Branch if rA is less or equal to 0, to the instruction located in the offset value of IMM. The target of the branch will be the instruction at address PC + IMM.

The mnemonic bleid will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA <= 0 then
    PC ← PC + sext(IMM)
else
    PC ← PC + 4
if D = 1 then
    allow following instruction to complete execution

```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “[imm,](#)” page 147 for details on using 32-bit immediate values.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

blt

Branch if Less Than

blt	rA, rB	Branch if Less Than
bltd	rA, rB	Branch if Less Than with Delay

1	0	0	1	1	1	D	0	0	1	0	rA	rB	0	0	0	0	0	0	0	0	0	0	
0						6						1		1		2						3	
												1		6		1						1	

Description

Branch if rA is less than 0, to the instruction located in the offset value of rB. The target of the branch will be the instruction at address PC + rB.

The mnemonic bltd will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA < 0 then
    PC ← PC + rB
else
    PC ← PC + 4
if D = 1 then
    allow following instruction to complete execution
    
```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

blti

Branch Immediate if Less Than

blti	rA, IMM	Branch Immediate if Less Than
bltid	rA, IMM	Branch Immediate if Less Than with Delay

1	0	1	1	1	1	D	0	0	1	0	rA	IMM
0						6					1	1
											1	6
												3
												1

Description

Branch if rA is less than 0, to the instruction located in the offset value of IMM. The target of the branch will be the instruction at address PC + IMM.

The mnemonic bltid will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA < 0 then
  PC ← PC + sext (IMM)
else
  PC ← PC + 4
if D = 1 then
  allow following instruction to complete execution

```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “[imm,](#)” page 147 for details on using 32-bit immediate values.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

bne

Branch if Not Equal

bne	rA, rB	Branch if Not Equal
bned	rA, rB	Branch if Not Equal with Delay

1	0	0	1	1	1	D	0	0	0	1	rA	rB	0	0	0	0	0	0	0	0	0	0	
0						6						1		1		2						3	
												1		6		1						1	

Description

Branch if rA not equal to 0, to the instruction located in the offset value of rB. The target of the branch will be the instruction at address PC + rB.

The mnemonic bned will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA ≠ 0 then
    PC ← PC + rB
else
    PC ← PC + 4
if D = 1 then
    allow following instruction to complete execution
    
```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

bnei

Branch Immediate if Not Equal

bnei	rA, IMM	Branch Immediate if Not Equal
bneid	rA, IMM	Branch Immediate if Not Equal with Delay

1	0	1	1	1	1	D	0	0	0	1	rA	IMM	
0						6					1	1	3
											1	6	1

Description

Branch if rA not equal to 0, to the instruction located in the offset value of IMM. The target of the branch will be the instruction at address PC + IMM.

The mnemonic bneid will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

If rA ≠ 0 then
    PC ← PC + sext (IMM)
else
    PC ← PC + 4
if D = 1 then
    allow following instruction to complete execution

```

Registers Altered

- PC

Latency

- 1 cycle (if branch is not taken)
- 2 cycles (if branch is taken and the D bit is set)
- 3 cycles (if branch is taken and the D bit is not set)

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “[imm,](#)” page 147 for details on using 32-bit immediate values.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

br

Unconditional Branch

br	rB	Branch
bra	rB	Branch Absolute
brd	rB	Branch with Delay
brad	rB	Branch Absolute with Delay
brld	rD, rB	Branch and Link with Delay
brald	rD, rB	Branch Absolute and Link with Delay

1 0 0 1 1 0	rD	D A L 0 0	rB	0 0 0 0 0 0 0 0 0 0
0	6	1	1	2
		1	6	1
				3
				1

Description

Branch to the instruction located at address determined by rB.

The mnemonics brld and brald will set the L bit. If the L bit is set, linking will be performed. The current value of PC will be stored in rD.

The mnemonics bra, brad and brald will set the A bit. If the A bit is set, it means that the branch is to an absolute value and the target is the value in rB, otherwise, it is a relative branch and the target will be PC + rB.

The mnemonics brd, brad, brld and brald will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction.

If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

Pseudocode

```

if L = 1 then
    (rD) ← PC
if A = 1 then
    PC ← (rB)
else
    PC ← PC + (rB)
    if D = 1 then
        allow following instruction to complete execution
    
```

Registers Altered

- rD
- PC

Latency

- 2 cycles (if the D bit is set)
- 3 cycles (if the D bit is not set)

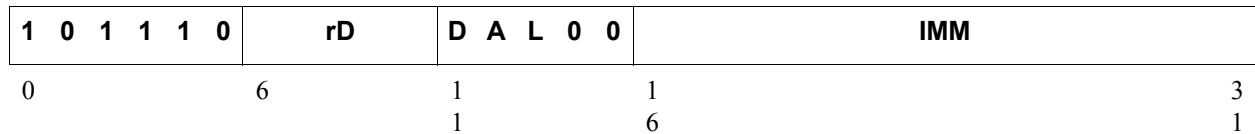
Note

The instructions `brl` and `bral` are not available. A delay slot must not be used by the following: `imm`, `branch`, or `break` instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

bri

Unconditional Branch Immediate

bri	IMM	Branch Immediate
brai	IMM	Branch Absolute Immediate
brid	IMM	Branch Immediate with Delay
braid	IMM	Branch Absolute Immediate with Delay
brlid	rD, IMM	Branch and Link Immediate with Delay
bralid	rD, IMM	Branch Absolute and Link Immediate with Delay



Description

Branch to the instruction located at address determined by IMM, sign-extended to 32 bits.

The mnemonics brlid and bralid will set the L bit. If the L bit is set, linking will be performed. The current value of PC will be stored in rD.

The mnemonics brai, braid and bralid will set the A bit. If the A bit is set, it means that the branch is to an absolute value and the target is the value in IMM, otherwise, it is a relative branch and the target will be PC + IMM.

The mnemonics brid, braid, brlid and bralid will set the D bit. The D bit determines whether there is a branch delay slot or not. If the D bit is set, it means that there is a delay slot and the instruction following the branch (for example, in the branch delay slot) is allowed to complete execution before executing the target instruction. If the D bit is not set, it means that there is no delay slot, so the instruction to be executed after the branch is the target instruction.

As a special case, when MicroBlaze is configured to use an MMU ($C_USE_MMU \geq 1$) and “bralid rD, 0x8” is used to perform a User Vector Exception, the Machine Status Register bits User Mode and Virtual Mode are cleared.

Pseudocode

```

if L = 1 then
    (rD) ← PC
if A = 1 then
    PC ← (IMM)
else
    PC ← PC + (IMM)
if D = 1 then
    allow following instruction to complete execution
if D = 1 and A = 1 and L = 1 and IMM = 0x8 then
    MSR[UMS] ← MSR[UM]
    MSR[VMS] ← MSR[VM]
    MSR[UM] ← 0
    MSR[VM] ← 0
    
```

Registers Altered

- rD
- PC
- MSR[UM], MSR[VM]

Latency

- 2 cycles (if the D bit is set)
- 3 cycles (if the D bit is not set)

Notes

The instructions brli and brali are not available.

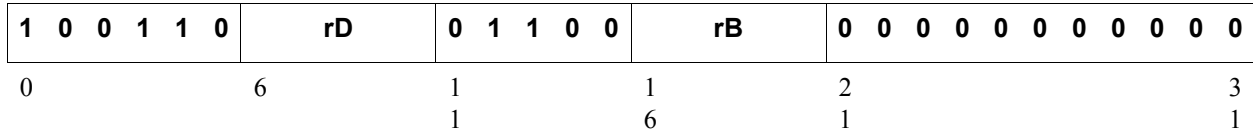
By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “[imm](#),” [page 147](#) for details on using 32-bit immediate values.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

brk

Break

brk rD, rB



Description

Branch and link to the instruction located at address value in rB. The current value of PC will be stored in rD. The BIP flag in the MSR will be set.

When MicroBlaze is configured to use an MMU (C_USE_MMU >= 1) this instruction is privileged. This means that if the instruction is attempted in User Mode (MSR[UM] = 1) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    (rD) ← PC
    PC ← (rB)
    MSR[BIP] ← 1
    
```

Registers Altered

- rD
- PC
- MSR[BIP]
- ESR[EC], in case a privileged instruction exception is generated

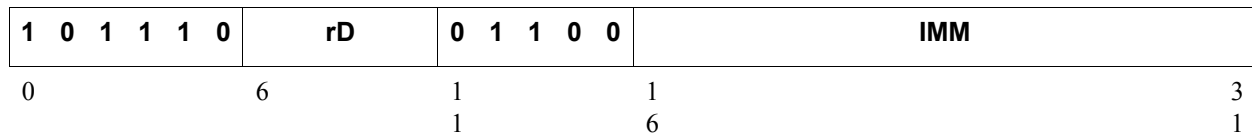
Latency

- 3 cycles

brki

Break Immediate

brki rD, IMM



Description

Branch and link to the instruction located at address value in IMM, sign-extended to 32 bits. The current value of PC will be stored in rD. The BIP flag in the MSR will be set.

When MicroBlaze is configured to use an MMU (`C_USE_MMU >= 1`) this instruction is privileged, except as a special case when “brki rD, 0x8” or “brki rD, 0x18” is used to perform a Software Break. This means that, apart from the special case, if the instruction is attempted in User Mode (`MSR[UM] = 1`) a Privileged Instruction exception occurs.

As a special case, when MicroBlaze is configured to use an MMU (`C_USE_MMU >= 1`) and “brki rD, 0x8” or “brki rD, 0x18” is used to perform a Software Break, the Machine Status Register bits User Mode and Virtual Mode are cleared.

Pseudocode

```

if MSR[UM] == 1 && IMM != 0x8 && IMM != 0x18 then
    ESR[EC] ← 00111
else
    (rD) ← PC
    PC ← sext(IMM)
    MSR[BIP] ← 1
    if IMM = 0x8 || IMM = 0x18 then
        MSR[UMS] ← MSR[UM]
        MSR[VMS] ← MSR[VM]
        MSR[UM] ← 0
        MSR[VM] ← 0

```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- PC
- MSR[BIP], MSR[UM], MSR[VM]
- ESR[EC], in case a privileged instruction exception is generated

Latency

- 3 cycles

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

bs

Barrel Shift

bsrl	rD, rA, rB	Barrel Shift Right Logical
bsra	rD, rA, rB	Barrel Shift Right Arithmetical
bsll	rD, rA, rB	Barrel Shift Left Logical

0	1	0	0	0	1	rD	rA	rB	S	T	0	0	0	0	0	0	0	0	0
0						6	1	1	2										3
							1	6	1										1

Description

Shifts the contents of register rA by the amount specified in register rB and puts the result in register rD.

The mnemonic bsll sets the S bit (Side bit). If the S bit is set, the barrel shift is done to the left. The mnemonics bsrl and bsra clear the S bit and the shift is done to the right.

The mnemonic bsra will set the T bit (Type bit). If the T bit is set, the barrel shift performed is Arithmetical. The mnemonics bsrl and bsll clear the T bit and the shift performed is Logical.

Pseudocode

```

if S = 1 then
    (rD) ← (rA) << (rB) [27:31]
else
    if T = 1 then
        if ((rB) [27:31]) ≠ 0 then
            (rD) [0:(rB) [27:31]-1] ← (rA) [0]
            (rD) [(rB) [27:31]:31] ← (rA) >> (rB) [27:31]
        else
            (rD) ← (rA)
    else
        (rD) ← (rA) >> (rB) [27:31]

```

Registers Altered

- rD

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

Note

These instructions are optional. To use them, MicroBlaze has to be configured to use barrel shift instructions (C_USE_BARREL=1).

bsi

Barrel Shift Immediate

bsrli	rD, rA, IMM	Barrel Shift Right Logical Immediate
bsrai	rD, rA, IMM	Barrel Shift Right Arithmetical Immediate
bslli	rD, rA, IMM	Barrel Shift Left Logical Immediate

0 1 1 0 0 1	rD	rA	0 0 0 0 0	S T 0 0 0 0	IMM
0	6	1	1	2	2
		1	6	1	7
					3
					1

Description

Shifts the contents of register rA by the amount specified by IMM and puts the result in register rD.

The mnemonic bsll sets the S bit (Side bit). If the S bit is set, the barrel shift is done to the left. The mnemonics bsrl and bsra clear the S bit and the shift is done to the right.

The mnemonic bsra will set the T bit (Type bit). If the T bit is set, the barrel shift performed is Arithmetical. The mnemonics bsrl and bsll clear the T bit and the shift performed is Logical.

Pseudocode

```

if S = 1 then
  (rD) ← (rA) << IMM
else
  if T = 1 then
    if IMM ≠ 0 then
      (rD) [0:IMM-1] ← (rA) [0]
      (rD) [IMM:31] ← (rA) >> IMM
    else
      (rD) ← (rA)
  else
    (rD) ← (rA) >> IMM

```

Registers Altered

- rD

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

Notes

These are not Type B Instructions. There is no effect from a preceding imm instruction.

These instructions are optional. To use them, MicroBlaze has to be configured to use barrel shift instructions (C_USE_BARREL=1).

cmp

Integer Compare

cmp	rD, rA, rB	compare rB with rA (signed)
cmpu	rD, rA, rB	compare rB with rA (unsigned)

0	0	0	1	0	1	rD	rA	rB	0	0	0	0	0	0	0	0	0	U	1
0						6	1	1	2										3
							1	6	1										1

Description

The contents of register rA is subtracted from the contents of register rB and the result is placed into register rD.

The MSB bit of rD is adjusted to shown true relation between rA and rB. If the U bit is set, rA and rB is considered unsigned values. If the U bit is clear, rA and rB is considered signed values.

Pseudocode

$$(rD) \leftarrow (rB) + (\overline{rA}) + 1$$

$$(rD) (MSB) \leftarrow (rA) > (rB)$$

Registers Altered

- rD

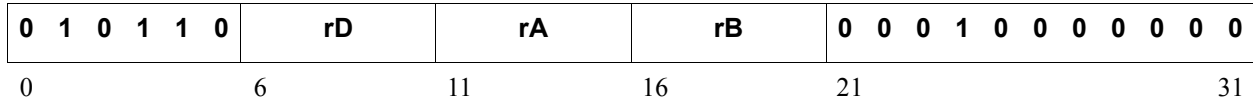
Latency

- 1 cycle

frsub

Reverse Floating Point Arithmetic Subtraction

frsub rD, rA, rB Reverse subtract



Description

The floating point value in rA is subtracted from the floating point value in rB and the result is placed into register rD.

Pseudocode

```

if isDnz(rA) or isDnz(rB) then
    (rD) ← 0xFFC00000
    FSR[DO] ← 1
    ESR[EC] ← 00110
else if (isSigNaN(rA) or isSigNaN(rB) or
        (isPosInfinite(rA) and isPosInfinite(rB)) or
        (isNegInfinite(rA) and isNegInfinite(rB))) then
    (rD) ← 0xFFC00000
    FSR[IO] ← 1
    ESR[EC] ← 00110
else if isQuietNaN(rA) or isQuietNaN(rB) then
    (rD) ← 0xFFC00000
else if isDnz((rB)-(rA)) then
    (rD) ← signZero((rB)-(rA))
    FSR[UF] ← 1
    ESR[EC] ← 00110
else if isNaN((rB)-(rA)) and then
    (rD) ← signInfinite((rB)-(rA))
    FSR[OF] ← 1
    ESR[EC] ← 00110
else
    (rD) ← (rB) - (rA)
    
```

Registers Altered

- rD, unless an FP exception is generated, in which case the register is unchanged
- ESR[EC], if an FP exception is generated
- FSR[IO,UF,OF,DO]

Latency

- 4 cycles with C_AREA_OPTIMIZED=0
- 6 cycles with C_AREA_OPTIMIZED=1

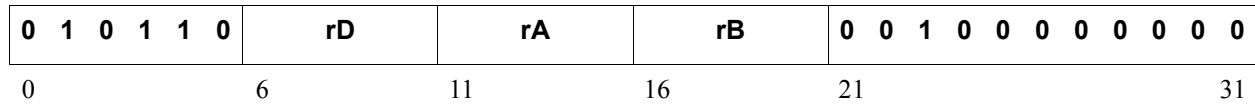
Note

This instruction is only available when the MicroBlaze parameter C_USE_FPU is greater than 0.

fmul

Floating Point Arithmetic Multiplication

fmul rD, rA, rB Multiply



Description

The floating point value in rA is multiplied with the floating point value in rB and the result is placed into register rD.

Pseudocode

```

if isDnz(rA) or isDnz(rB) then
    (rD) ← 0xFFC00000
    FSR[DO] ← 1
    ESR[EC] ← 00110
else
    if isSigNaN(rA) or isSigNaN(rB) or (isZero(rA) and isInfinite(rB)) or
       (isZero(rB) and isInfinite(rA)) then
        (rD) ← 0xFFC00000
        FSR[IO] ← 1
        ESR[EC] ← 00110
    else if isQuietNaN(rA) or isQuietNaN(rB) then
        (rD) ← 0xFFC00000
    else if isDnz((rB)*(rA)) then
        (rD) ← signZero((rA)*(rB))
        FSR[UF] ← 1
        ESR[EC] ← 00110
    else if isNaN((rB)*(rA)) and then
        (rD) ← signInfinite((rB)*(rA))
        FSR[OF] ← 1
        ESR[EC] ← 00110
    else
        (rD) ← (rB) * (rA)

```

Registers Altered

- rD, unless an FP exception is generated, in which case the register is unchanged
- ESR[EC], if an FP exception is generated
- FSR[IO,UF,OF,DO]

Latency

- 4 cycles with C_AREA_OPTIMIZED=0
- 6 cycles with C_AREA_OPTIMIZED=1

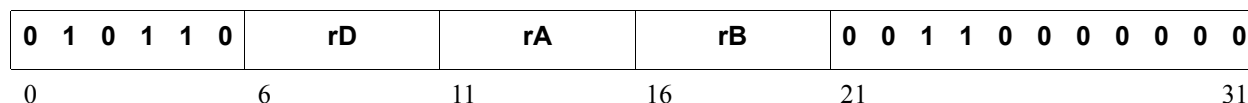
Note

This instruction is only available when the MicroBlaze parameter C_USE_FPU is greater than 0.

fdiv

Floating Point Arithmetic Division

fdiv rD, rA, rB Divide



Description

The floating point value in rB is divided by the floating point value in rA and the result is placed into register rD.

Pseudocode

```

if isDnz(rA) or isDnz(rB) then
    (rD) ← 0xFFC00000
    FSR[DO] ← 1
    ESR[EC] ← 00110
else
    if isSigNaN(rA) or isSigNaN(rB) or (isZero(rA) and isZero(rB)) or
       (isInfinite(rA) and isInfinite(rB)) then
        (rD) ← 0xFFC00000
        FSR[IO] ← 1
        ESR[EC] ← 00110
    else if isQuietNaN(rA) or isQuietNaN(rB) then
        (rD) ← 0xFFC00000
    else if isZero(rA) and not isInfinite(rB) then
        (rD) ← signInfinite((rB)/(rA))
        FSR[DZ] ← 1
        ESR[EC] ← 00110
    else if isDnz((rB)/(rA)) then
        (rD) ← signZero((rA)/(rB))
        FSR[UF] ← 1
        ESR[EC] ← 00110
    else if isNaN((rB)/(rA)) and then
        (rD) ← signInfinite((rB)/(rA))
        FSR[OF] ← 1
        ESR[EC] ← 00110
    else
        (rD) ← (rB) / (rA)
    
```

Registers Altered

- rD, unless an FP exception is generated, in which case the register is unchanged
- ESR[EC], if an FP exception is generated
- FSR[IO,UF,OF,DO,DZ]

Latency

- 28 cycles with C_AREA_OPTIMIZED=0, 30 cycles with C_AREA_OPTIMIZED=1

Note

This instruction is only available when the MicroBlaze parameter C_USE_FPU is greater than 0.

fcmp

Floating Point Number Comparison

fcmp.un	rD, rA, rB	Unordered floating point comparison
fcmp.lt	rD, rA, rB	Less-than floating point comparison
fcmp.eq	rD, rA, rB	Equal floating point comparison
fcmp.le	rD, rA, rB	Less-or-Equal floating point comparison
fcmp.gt	rD, rA, rB	Greater-than floating point comparison
fcmp.ne	rD, rA, rB	Not-Equal floating point comparison
fcmp.ge	rD, rA, rB	Greater-or-Equal floating point comparison

0	1	0	1	1	0	rD	rA	rB	0	1	0	0	OpSel	0	0	0	0
0						6	11	16	21	25	28	31					

Description

The floating point value in rB is compared with the floating point value in rA and the comparison result is placed into register rD. The `OpSel` field in the instruction code determines the type of comparison performed.

Pseudocode

```

if isDnz(rA) or isDnz(rB) then
    (rD) ← 0
    FSR[DO] ← 1
    ESR[EC] ← 00110
else
    {read out behavior from Table 4-2}

```

Registers Altered

- rD, unless an FP exception is generated, in which case the register is unchanged
- ESR[EC], if an FP exception is generated
- FSR[IO,DO]

Latency

- 1 cycle with `C_AREA_OPTIMIZED=0`
- 3 cycles with `C_AREA_OPTIMIZED=1`

Note

These instructions are only available when the MicroBlaze parameter `C_USE_FPU` is greater than 0.

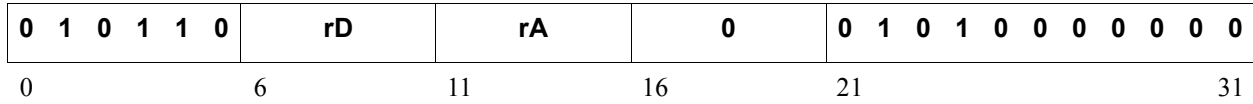
[Table 4-2, page 138](#) lists the floating point comparison operations.

Table 4-2: Floating Point Comparison Operation

Comparison Type		Operand Relationship			
Description	OpSel	(rB) > (rA)	(rB) < (rA)	(rB) = (rA)	isNaN(rA) or isNaN(rB)
Unordered	000	(rD) ← 0	(rD) ← 0	(rD) ← 0	(rD) ← 1
Less-than	001	(rD) ← 0	(rD) ← 1	(rD) ← 0	(rD) ← 0 FSR[IO] ← 1 ESR[EC] ← 00110
Equal	010	(rD) ← 0	(rD) ← 0	(rD) ← 1	(rD) ← 0
Less-or-equal	011	(rD) ← 0	(rD) ← 1	(rD) ← 1	(rD) ← 0 FSR[IO] ← 1 ESR[EC] ← 00110
Greater-than	100	(rD) ← 1	(rD) ← 0	(rD) ← 0	(rD) ← 0 FSR[IO] ← 1 ESR[EC] ← 00110
Not-equal	101	(rD) ← 1	(rD) ← 1	(rD) ← 0	(rD) ← 1
Greater-or-equal	110	(rD) ← 1	(rD) ← 0	(rD) ← 1	(rD) ← 0 FSR[IO] ← 1 ESR[EC] ← 00110

flt**Floating Point Convert Integer to Float**

flt rD, rA

**Description**

Converts the signed integer in register rA to floating point and puts the result in register rD. This is a 32-bit rounding signed conversion that will produce a 32-bit floating point result.

Pseudocode

```
(rD) ← float ((rA))
```

Registers Altered

- rD

Latency

- 4 cycles with C_AREA_OPTIMIZED=0
- 6 cycles with C_AREA_OPTIMIZED=1

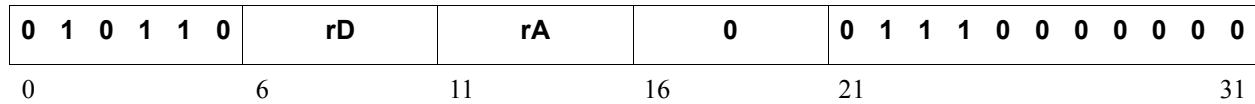
Note

This instruction is only available when the MicroBlaze parameter C_USE_FPU is set to 2.

fsqrt

Floating Point Arithmetic Square Root

fsqrt rD, rA Square Root



Description

Performs a floating point square root on the value in rA and puts the result in register rD.

Pseudocode

```

if isDnz(rA) then
  (rD) ← 0xFFC00000
  FSR[DO] ← 1
  ESR[EC] ← 00110
else if isSigNaN(rA) then
  (rD) ← 0xFFC00000
  FSR[IO] ← 1
  ESR[EC] ← 00110
else if isQuietNaN(rA) then
  (rD) ← 0xFFC00000
else if (rA) < 0 then
  (rD) ← 0xFFC00000
  FSR[IO] ← 1
  ESR[EC] ← 00110
else if (rA) = -0 then
  (rD) ← -0
else
  (rD) ← sqrt ((rA))

```

Registers Altered

- rD, unless an FP exception is generated, in which case the register is unchanged
- ESR[EC], if an FP exception is generated
- FSR[IO,UF,OF,DO]

Latency

- 27 cycles with C_AREA_OPTIMIZED=0
- 29 cycles with C_AREA_OPTIMIZED=1

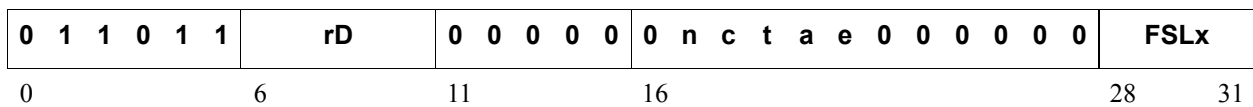
Note

This instruction is only available when the MicroBlaze parameter C_USE_FPU is set to 2.

get

get from fsl interface

<i>tnaaget</i>	rD, FSLx	get data from FSL x <i>t</i> = test-only <i>n</i> = non-blocking <i>e</i> = exception if control bit set <i>a</i> = atomic
<i>tnecaget</i>	rD, FSLx	get control from FSL x <i>t</i> = test-only <i>n</i> = non-blocking <i>e</i> = exception if control bit not set <i>a</i> = atomic



Description

MicroBlaze will read from the FSLx interface and place the result in register rD.

The get instruction has 32 variants.

The blocking versions (when ‘n’ bit is ‘0’) will stall microblaze until the data from the FSL interface is valid. The non-blocking versions will not stall microblaze and will set carry to ‘0’ if the data was valid and to ‘1’ if the data was invalid. In case of an invalid access the destination register contents is undefined.

All data get instructions (when ‘c’ bit is ‘0’) expect the control bit from the FSL interface to be ‘0’. If this is not the case, the instruction will set MSR[FSL_Error] to ‘1’. All control get instructions (when ‘c’ bit is ‘1’) expect the control bit from the FSL interface to be ‘1’. If this is not the case, the instruction will set MSR[FSL_Error] to ‘1’.

The exception versions (when ‘e’ bit is ‘1’) will generate an exception if there is a control bit mismatch. In this case ESR is updated with EC set to the exception cause and ESS set to the FSL index. The target register, rD, is not updated when an exception is generated, instead the FSL data is stored in EDR.

The test versions (when ‘t’ bit is ‘1’) will be handled as the normal case, except that the read signal to the FSL link is not asserted.

Atomic versions (when ‘a’ bit is ‘1’) are not interruptible. This means that a sequence of atomic FSL instructions can be grouped together without an interrupt breaking the program flow. However, note that exceptions may still occur.

When MicroBlaze is configured to use an MMU (C_USE_MMU >= 1) these instructions are privileged. This means that if these instructions are attempted in User Mode (MSR[UM]=1) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    (rD) ← FSLx
    if (n = 1) then
        MSR[Carry] ← not (FSLx Exists bit)
    if (FSLx Control bit ≠ c) then
        MSR[FSL_Error] ← 1
    if (e = 1) then
        ESR[EC] ← 00000
        ESR[ESS] ← instruction bits [28:31]
        EDR ← FSLx

```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[FSL_Error]
- MSR[Carry]
- ESR[EC], in case an FSL exception or a privileged instruction exception is generated
- ESR[ESS], in case an FSL exception is generated
- EDR, in case an FSL exception is generated

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

The blocking versions of this instruction will stall the pipeline of MicroBlaze until the instruction can be completed. Interrupts are served when the parameter C_USE_EXTENDED_FSL_INSTR is set to 1, and the instruction is not atomic.

Note

For non-blocking versions, an rsubc instruction can be used to decrement an index variable.

The 'e' bit does not have any effect unless C_FSL_EXCEPTION is set to 1.

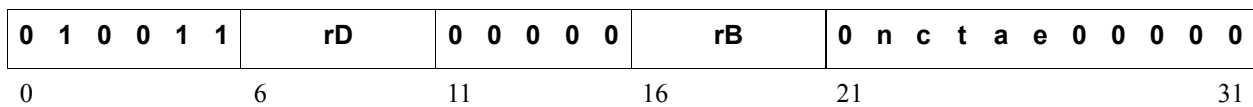
These instructions are only available when the MicroBlaze parameter C_FSL_LINKS is greater than 0.

The extended instructions (exception, test and atomic versions) are only available when the MicroBlaze parameter C_USE_EXTENDED_FSL_INSTR is set to 1.

getd

get from fsl interface dynamic

<i>tnegatd</i>	rD, rB	get data from FSL rB[28:31] <i>t</i> = test-only <i>n</i> = non-blocking <i>e</i> = exception if control bit set <i>a</i> = atomic
<i>tnecatd</i>	rD, rB	get control from FSL rB[28:31] <i>t</i> = test-only <i>n</i> = non-blocking <i>e</i> = exception if control bit not set <i>a</i> = atomic



Description

MicroBlaze will read from the FSL interface defined by the four least significant bits in rB and place the result in register rD.

The getd instruction has 32 variants.

The blocking versions (when ‘n’ bit is ‘0’) will stall microblaze until the data from the FSL interface is valid. The non-blocking versions will not stall microblaze and will set carry to ‘0’ if the data was valid and to ‘1’ if the data was invalid. In case of an invalid access the destination register contents is undefined.

All data get instructions (when ‘c’ bit is ‘0’) expect the control bit from the FSL interface to be ‘0’. If this is not the case, the instruction will set MSR[FSL_Error] to ‘1’. All control get instructions (when ‘c’ bit is ‘1’) expect the control bit from the FSL interface to be ‘1’. If this is not the case, the instruction will set MSR[FSL_Error] to ‘1’.

The exception versions (when ‘e’ bit is ‘1’) will generate an exception if there is a control bit mismatch. In this case ESR is updated with EC set to the exception cause and ESS set to the FSL index. The target register, rD, is not updated when an exception is generated, instead the FSL data is stored in EDR.

The test versions (when ‘t’ bit is ‘1’) will be handled as the normal case, except that the read signal to the FSL link is not asserted.

Atomic versions (when ‘a’ bit is ‘1’) are not interruptible. This means that a sequence of atomic FSL instructions can be grouped together without an interrupt breaking the program flow. However, note that exceptions may still occur.

When MicroBlaze is configured to use an MMU (C_USE_MMU >= 1) these instructions are privileged. This means that if these instructions are attempted in User Mode (MSR[UM] = 1) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    (rD) ← (FSL rB[28:31])
    if (n = 1) then
        MSR[Carry] ← not (FSL rB[28:31] Exists bit)
    if (FSL rB[28:31] Control bit ≠ c) then
        MSR[FSL_Error] ← 1
        if (e = 1) then
            ESR[EC] ← 00000
            ESR[ESS] ← rB[28:31]
            EDR ← (FSL rB[28:31])

```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[FSL_Error]
- MSR[Carry]
- ESR[EC], in case an FSL exception or a privileged instruction exception is generated
- ESR[ESS], in case an FSL exception is generated
- EDR, in case an FSL exception is generated

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

The blocking versions of this instruction will stall the pipeline of MicroBlaze until the instruction can be completed. Interrupts are served unless the instruction is atomic, which ensures that the instruction cannot be interrupted.

Note

For non-blocking versions, an rsubc instruction can be used to decrement an index variable.

The 'e' bit does not have any effect unless C_FSL_EXCEPTION is set to 1.

These instructions are only available when the MicroBlaze parameter C_FSL_LINKS is greater than 0 and the parameter C_USE_EXTENDED_FSL_INSTR is set to 1.

idiv

Integer Divide

idiv	rD, rA, rB	divide rB by rA (signed)
idivu	rD, rA, rB	divide rB by rA (unsigned)

0	1	0	0	1	0	rD	rA	rB	0	0	0	0	0	0	0	0	U	0
0						6	1	1	2						3			
						1	6	1							1			

Description

The contents of register rB is divided by the contents of register rA and the result is placed into register rD.

If the U bit is set, rA and rB is considered unsigned values. If the U bit is clear, rA and rB is considered signed values

If the value of rA is 0, the divide_by_zero bit in MSR will be set and the value in rD will be 0, unless an exception is generated.

Pseudocode

```

if (rA) = 0 then
    (rD)    <- 0
    MSR[DZ] <- 1
    ESR[EC] <- 00101
else
    (rD) ← (rB) / (rA)
    
```

Registers Altered

- rD, unless “Divide by zero” exception is generated, in which case the register is unchanged
- MSR[Divide_By_Zero], if the value in rA is zero
- ESR[EC], if the value in rA is zero

Latency

- 1 cycle if (rA) = 0, otherwise 32 cycles with C_AREA_OPTIMIZED=0
- 1 cycle if (rA) = 0, otherwise 34 cycles with C_AREA_OPTIMIZED=1

Note

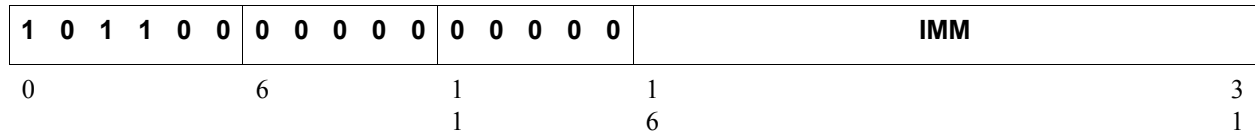
This instruction is only valid if MicroBlaze is configured to use a hardware divider (C_USE_DIV = 1).

imm

Immediate

imm

IMM



Description

The instruction `imm` loads the IMM value into a temporary register. It also locks this value so it can be used by the following instruction and form a 32-bit immediate value.

The instruction `imm` is used in conjunction with Type B instructions. Since Type B instructions have only a 16-bit immediate value field, a 32-bit immediate value cannot be used directly. However, 32-bit immediate values can be used in MicroBlaze. By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an `imm` instruction. The `imm` instruction locks the 16-bit IMM value temporarily for the next instruction. A Type B instruction that immediately follows the `imm` instruction will then form a 32-bit immediate value from the 16-bit IMM value of the `imm` instruction (upper 16 bits) and its own 16-bit immediate value field (lower 16 bits). If no Type B instruction follows the `imm` instruction, the locked value gets unlocked and becomes useless.

Latency

- 1 cycle

Notes

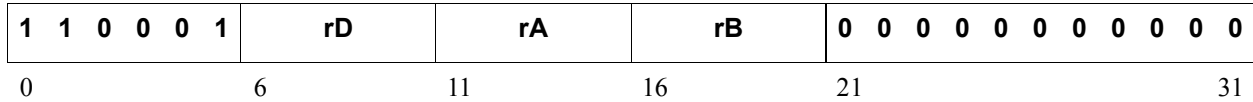
The `imm` instruction and the Type B instruction following it are atomic; consequently, no interrupts are allowed between them.

The assembler provided by Xilinx automatically detects the need for `imm` instructions. When a 32-bit IMM value is specified in a Type B instruction, the assembler converts the IMM value to a 16-bit one to assemble the instruction and inserts an `imm` instruction before it in the executable file.

lhu

Load Halfword Unsigned

lhu rD, rA, rB



Description

Loads a halfword (16 bits) from the halfword aligned memory location that results from adding the contents of registers rA and rB. The data is placed in the least significant halfword of register rD and the most significant halfword in rD is cleared.

A data TLB miss exception occurs if virtual protected mode is enabled, and a valid translation entry corresponding to the address is not found in the TLB.

A data storage exception occurs if access is prevented by a no-access-allowed zone protection. This only applies to accesses with user mode and virtual protected mode enabled.

An unaligned data access exception occurs if the least significant bit in the address is not zero.

Pseudocode

```

Addr ← (rA) + (rB)
if TLB_Miss(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10010; ESR[S] ← 0
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Access_Protected(Addr) and MSR[UM] == 1 and MSR[VM] == 1 then
    ESR[EC] ← 10000; ESR[S] ← 0; ESR[DIZ] ← 1
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Addr[31] != 0 then
    ESR[EC] ← 00001; ESR[W] ← 0; ESR[S] ← 0; ESR[Rx] ← rD
else
    (rD)[16:31] ← Mem(Addr)
    (rD)[0:15] ← 0
    
```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[UM], MSR[VM], MSR[UMS], MSR[VMS], if a TLB miss exception or a data storage exception is generated
- ESR[EC], ESR[S], if an exception is generated
- ESR[DIZ], if a data storage exception is generated
- ESR[W], ESR[Rx], if an unaligned data access exception is generated

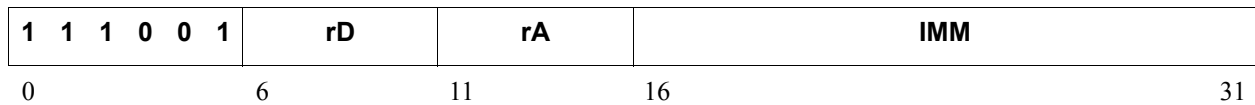
Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

lhui

Load Halfword Unsigned Immediate

lhui rD, rA, IMM



Description

Loads a halfword (16 bits) from the halfword aligned memory location that results from adding the contents of register rA and the value in IMM, sign-extended to 32 bits. The data is placed in the least significant halfword of register rD and the most significant halfword in rD is cleared.

A data TLB miss exception occurs if virtual protected mode is enabled, and a valid translation entry corresponding to the address is not found in the TLB. A data storage exception occurs if access is prevented by a no-access-allowed zone protection. This only applies to accesses with user mode and virtual protected mode enabled. An unaligned data access exception occurs if the least significant bit in the address is not zero.

Pseudocode

```

Addr ← (rA) + sext(IMM)
if TLB_Miss(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10010; ESR[S] ← 0
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Access_Protected(Addr) and MSR[UM] == 1 and MSR[VM] == 1 then
    ESR[EC] ← 10000; ESR[S] ← 0; ESR[DIZ] ← 1
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Addr[31] != 0 then
    ESR[EC] ← 00001; ESR[W] ← 0; ESR[S] ← 0; ESR[Rx] ← rD
else
    (rD)[16:31] ← Mem(Addr)
    (rD)[0:15] ← 0

```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[UM], MSR[VM], MSR[UMS], MSR[VMS], if a TLB miss exception or a data storage exception is generated
- ESR[EC], ESR[S], if an exception is generated
- ESR[DIZ], if a data storage exception is generated
- ESR[W], ESR[Rx], if an unaligned data access exception is generated

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

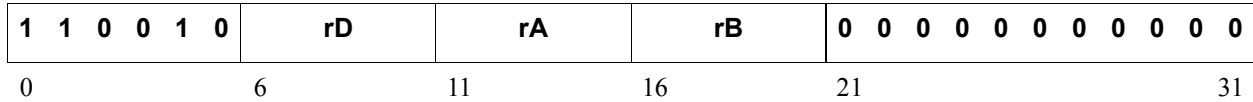
Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

lw

Load Word

lw rD, rA, rB



Description

Loads a word (32 bits) from the word aligned memory location that results from adding the contents of registers rA and rB. The data is placed in register rD.

A data TLB miss exception occurs if virtual protected mode is enabled, and a valid translation entry corresponding to the address is not found in the TLB.

A data storage exception occurs if access is prevented by a no-access-allowed zone protection. This only applies to accesses with user mode and virtual protected mode enabled.

An unaligned data access exception occurs if the two least significant bits in the address are not zero.

Pseudocode

```

Addr ← (rA) + (rB)
if TLB_Miss(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10010; ESR[S] ← 0
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Access_Protected(Addr) and MSR[UM] == 1 and MSR[VM] == 1 then
    ESR[EC] ← 10000; ESR[S] ← 0; ESR[DIZ] ← 1
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Addr[30:31] != 0 then
    ESR[EC] ← 00001; ESR[W] ← 1; ESR[S] ← 0; ESR[Rx] ← rD
else
    (rD) ← Mem(Addr)
    
```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[UM], MSR[VM], MSR[UMS], MSR[VMS], if a TLB miss exception or a data storage exception is generated
- ESR[EC], ESR[S], if an exception is generated
- ESR[DIZ], if a data storage exception is generated
- ESR[W], ESR[Rx], if an unaligned data access exception is generated

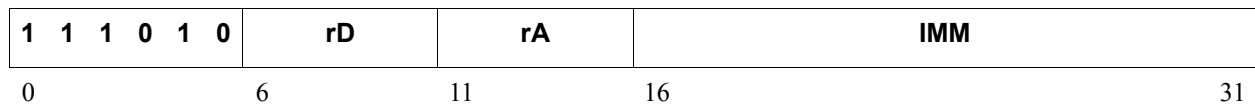
Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

lwi

Load Word Immediate

lwi rD, rA, IMM



Description

Loads a word (32 bits) from the word aligned memory location that results from adding the contents of register rA and the value IMM, sign-extended to 32 bits. The data is placed in register rD. A data TLB miss exception occurs if virtual protected mode is enabled, and a valid translation entry corresponding to the address is not found in the TLB. A data storage exception occurs if access is prevented by a no-access-allowed zone protection. This only applies to accesses with user mode and virtual protected mode enabled. An unaligned data access exception occurs if the two least significant bits in the address are not zero.

Pseudocode

```

Addr ← (rA) + sext(IMM)
if TLB_Miss(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10010; ESR[S] ← 0
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Access_Protected(Addr) and MSR[UM] == 1 and MSR[VM] == 1 then
    ESR[EC] ← 10000; ESR[S] ← 0; ESR[DIZ] ← 1
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Addr[30:31] != 0 then
    ESR[EC] ← 00001; ESR[W] ← 1; ESR[S] ← 0; ESR[Rx] ← rD
else
    (rD) ← Mem(Addr)

```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[UM], MSR[VM], MSR[UMS], MSR[VMS], if a TLB miss exception or a data storage exception is generated
- ESR[EC], ESR[S], if an exception is generated
- ESR[DIZ], if a data storage exception is generated
- ESR[W], ESR[Rx], if an unaligned data access exception is generated

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

Notes

To refer to special purpose registers in assembly language, use `rpc` for PC, `rmsr` for MSR, `rear` for EAR, `resr` for ESR, `rfsr` for FSR, `rbtr` for BTR, `redr` for EDR, `rpdr` for PID, `rzpr` for ZPR, `rtlblo` for TLBLO, `rtlbhi` for TLBHI, `rtlbn` for TLBN, and `rpvr0 - rpvr11` for PVR0 - PVR11.

The value read from MSR may not include effects of the immediately preceding instruction (dependent on pipeline stall behavior). A NOP should be inserted before the MFS instruction to guarantee correct MSR value.

EAR, ESR and BTR are only valid as operands when at least one of the MicroBlaze `C_*_EXCEPTION` parameters are set to 1.

EDR is only valid as operand when the parameter `C_FSL_EXCEPTION` is set to 1 and the parameter `C_FSL_LINKS` is greater than 0.

FSR is only valid as an operand when the `C_USE_FPU` parameter is greater than 0.

PID, ZPR, TLBLO and TLBHI are only valid as operands when the parameter `C_USE_MMU` > 1 and the parameter `C_MMU_TLB_ACCESS` = 1 or 3.

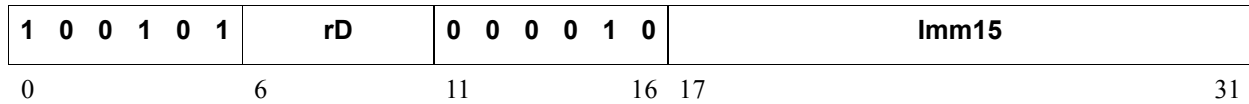
TLBN is only valid as operand when the parameter `C_USE_MMU` > 1 and the parameter `C_MMU_TLB_ACCESS` > 0.

PVR0 is only valid as an operand when `C_PVR` is 1 or 2, and PVR1 - PVR11 are only valid as operands when `C_PVR` is set to 2.

msrclr

Read MSR and clear bits in MSR

msrclr rD, Imm



Description

Copies the contents of the special purpose register MSR into register rD.

Bit positions in the IMM value that are 1 are cleared in the MSR. Bit positions that are 0 in the IMM value are left untouched.

When MicroBlaze is configured to use an MMU (`C_USE_MMU >= 1`) this instruction is privileged for all IMM values except those only affecting C. This means that if the instruction is attempted in User Mode (`MSR [UM] = 1`) in this case a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 && IMM != 0x4 then
    ESR[EC] ← 00111
else
    (rD) ← (MSR)
    (MSR) ← (MSR) ^ (IMM)
    
```

Registers Altered

- rD
- MSR
- ESR[EC], in case a privileged instruction exception is generated

Latency

- 1 cycle

Note

MSRCLR will affect the Carry bit immediately while the remaining bits will take effect one cycle after the instruction has been executed.

The immediate values has to be less than 2^{15} . Only bits 17 to 31 of the MSR can be cleared.

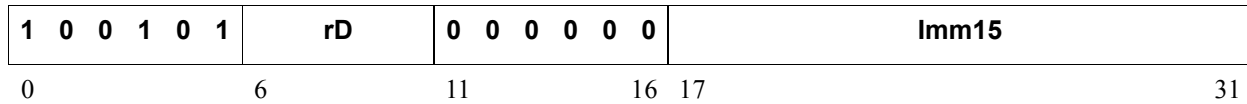
This instruction is only available when the parameter `C_USE_MSR_INSTR` is set to 1.

When clearing `MSR[VM]` the instruction must always be followed by a synchronizing branch instruction, for example BRI 4.

msrset

Read MSR and set bits in MSR

msrset rD, Imm



Description

Copies the contents of the special purpose register MSR into register rD.

Bit positions in the IMM value that are 1 are set in the MSR. Bit positions that are 0 in the IMM value are left untouched.

When MicroBlaze is configured to use an MMU (`C_USE_MMU >= 1`) this instruction is privileged for all IMM values except those only affecting C. This means that if the instruction is attempted in User Mode (`MSR[UM] = 1`) in this case a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 && IMM != 0x4 then
    ESR[EC] ← 00111
else
    (rD) ← (MSR)
    (MSR) ← (MSR) ∨ (IMM)

```

Registers Altered

- rD
- MSR
- ESR[EC], in case a privileged instruction exception is generated

Latency

- 1 cycle

Note

MSRSET will affect the Carry bit immediately while the remaining bits will take effect one cycle after the instruction has been executed.

The immediate values has to be less than 2^{15} . Only bits 17 to 31 of the MSR can be set.

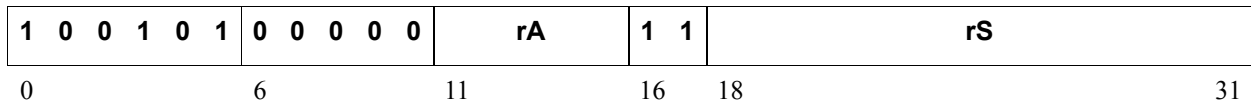
This instruction is only available when the parameter `C_USE_MSR_INSTR` is set to 1.

When setting `MSR[VM]` the instruction must always be followed by a synchronizing branch instruction, for example BRI 4.

mts

Move To Special Purpose Register

mts rS, rA



Description

Copies the contents of register rD into the special purpose register rS. The special purpose registers TLBLO and TLBHI are used to copy to the Unified TLB entry indexed by TLBX.

When MicroBlaze is configured to use an MMU (C_USE_MMU >= 1) this instruction is privileged. This means that if the instruction is attempted in User Mode (MSR [UM] = 1) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    switch (rS)
        case 0x0001 : MSR ← (rA)
        case 0x0007 : FSR ← (rA)
        case 0x1000 : PID ← (rA)
        case 0x1001 : ZPR ← (rA)
        case 0x1002 : TLBX ← (rA)
        case 0x1003 : TLBLO ← (rA)
        case 0x1004 : TLBHI ← (rA)
        case 0x1005 : TLBSX ← (rA)
    
```

Registers Altered

- rS
- ESR[EC], in case a privileged instruction exception is generated

Latency

- 1 cycle

Notes

When writing MSR using MTS, the Carry bit takes effect immediately while the remaining bits take effect one cycle after the instruction has been executed.

To refer to special purpose registers in assembly language, use rmsr for MSR, rfsr for FSR, rpid for PID, rzpr for ZPR, rtlblo for TLBLO, rtlbhi for TLBHI, rtlbx for TLBX, and rtlbsx for TLBSX.

The PC, ESR, EAR, BTR, EDR and PVR0 - PVR11 cannot be written by the MTS instruction.

The FSR is only valid as a destination if the MicroBlaze parameter C_USE_FPU is greater than 0.

PID, ZPR and TLBSX are only valid as destinations when the parameter C_USE_MMU > 1 and the parameter C_MMU_TLB_ACCESS > 1. TLBLO, TLBHI and TLBX are only valid as destinations when the parameter C_USE_MMU > 1.

When changing MSR[VM] or PID the instruction must always be followed by a synchronizing branch instruction, for example BRI 4.

mul

Multiply

mul rD, rA, rB

0	1	0	0	0	0	rD	rA	rB	0	0	0	0	0	0	0	0	0	0
0						6	1	1	2									3
							1	6	1									1

Description

Multiplies the contents of registers rA and rB and puts the result in register rD. This is a 32-bit by 32-bit multiplication that will produce a 64-bit result. The least significant word of this value is placed in rD. The most significant word is discarded.

Pseudocode

$$(rD) \leftarrow \text{LSW}((rA) \times (rB))$$

Registers Altered

- rD

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 3 cycles with C_AREA_OPTIMIZED=1

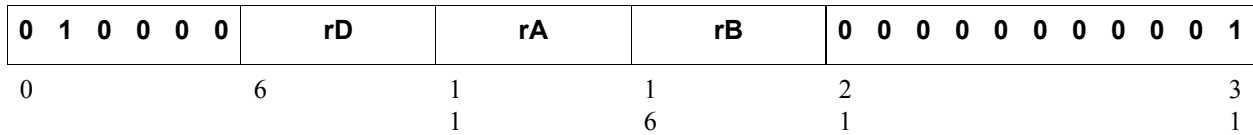
Note

This instruction is only valid if the target architecture has multiplier primitives, and if present, the MicroBlaze parameter C_USE_HW_MUL is greater than 0.

mulh

Multiply High

mulh rD, rA, rB



Description

Multiplies the contents of registers rA and rB and puts the result in register rD. This is a 32-bit by 32-bit signed multiplication that will produce a 64-bit result. The most significant word of this value is placed in rD. The least significant word is discarded.

Pseudocode

$$(rD) \leftarrow \text{MSW}((rA) \times (rB)), \text{ signed}$$

Registers Altered

- rD

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 3 cycles with C_AREA_OPTIMIZED=1

Note

This instruction is only valid if the target architecture has multiplier primitives, and if present, the MicroBlaze parameter C_USE_HW_MUL is set to 2.

When MULH is used, bit 30 and 31 in the MUL instruction must be zero to distinguish between the two instructions. In previous versions of MicroBlaze, these bits were defined as zero, but the actual values were not relevant.

mulhu

Multiply High Unsigned

mulhu rD, rA, rB

0 1 0 0 0 0	rD	rA	rB	0 0 0 0 0 0 0 0 0 0 1 1
0	6	1	1	2
		1	6	1
				3
				1

Description

Multiplies the contents of registers rA and rB and puts the result in register rD. This is a 32-bit by 32-bit unsigned multiplication that will produce a 64-bit unsigned result. The most significant word of this value is placed in rD. The least significant word is discarded.

Pseudocode

$$(rD) \leftarrow \text{MSW}((rA) \times (rB)), \text{ unsigned}$$

Registers Altered

- rD

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 3 cycles with C_AREA_OPTIMIZED=1

Note

This instruction is only valid if the target architecture has multiplier primitives, and if present, the MicroBlaze parameter C_USE_HW_MUL is set to 2.

When MULHU is used, bit 30 and 31 in the MUL instruction must be zero to distinguish between the two instructions. In previous versions of MicroBlaze, these bits were defined as zero, but the actual values were not relevant.

mulhsu Multiply High Signed Unsigned

mulhsu rD, rA, rB

0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0					
						rD						rA						rB																	
0						6						1						1						2						3					
												1						6						1						1					

Description

Multiplies the contents of registers rA and rB and puts the result in register rD. This is a 32-bit signed by 32-bit unsigned multiplication that will produce a 64-bit signed result. The most significant word of this value is placed in rD. The least significant word is discarded.

Pseudocode

$(rD) \leftarrow \text{MSW}((rA), \text{signed} \times (rB), \text{unsigned}), \text{signed}$

Registers Altered

- rD

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 3 cycles with C_AREA_OPTIMIZED=1

Note

This instruction is only valid if the target architecture has multiplier primitives, and if present, the MicroBlaze parameter C_USE_HW_MUL is set to 2.

When MULHSU is used, bit 30 and 31 in the MUL instruction must be zero to distinguish between the two instructions. In previous versions of MicroBlaze, these bits were defined as zero, but the actual values were not relevant.

mul

Multiply Immediate

mul rD, rA, IMM

0	1	1	0	0	0	rD	rA	IMM
0					6	1	1	3
						1	6	1

Description

Multiplies the contents of registers rA and the value IMM, sign-extended to 32 bits; and puts the result in register rD. This is a 32-bit by 32-bit multiplication that will produce a 64-bit result. The least significant word of this value is placed in rD. The most significant word is discarded.

Pseudocode

$$(rD) \leftarrow \text{LSW} (rA \times \text{sext} (IMM))$$

Registers Altered

- rD

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 3 cycles with C_AREA_OPTIMIZED=1

Notes

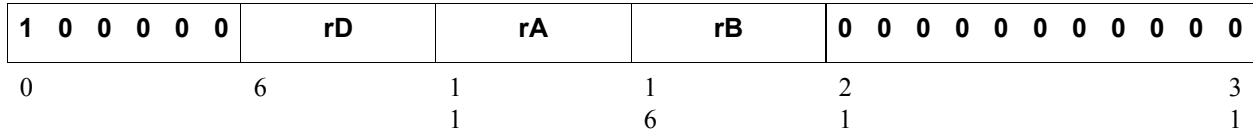
By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “[imm](#),” [page 147](#) for details on using 32-bit immediate values.

This instruction is only valid if the target architecture has multiplier primitives, and if present, the MicroBlaze parameter C_USE_HW_MUL is greater than 0.

or

Logical OR

or rD, rA, rB



Description

The contents of register rA are ORed with the contents of register rB; the result is placed into register rD.

Pseudocode

$$(rD) \leftarrow (rA) \vee (rB)$$

Registers Altered

- rD

Latency

- 1 cycle

ori

Logical OR with Immediate

ori rD, rA, IMM

1	0	1	0	0	0	rD	rA	IMM
0					6	1	1	3
						1	6	1

Description

The contents of register rA are ORed with the extended IMM field, sign-extended to 32 bits; the result is placed into register rD.

Pseudocode

$$(rD) \leftarrow (rA) \vee (IMM)$$

Registers Altered

- rD

Latency

- 1 cycle

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

pcmpbf

Pattern Compare Byte Find

pcmpbf rD, rA, rB bitwise comparison returning position of first match

1	0	0	0	0	0	rD	rA	rB	1	0	0	0	0	0	0	0	0	0	0	
0						6	1	1	2											3
							1	6	1											1

Description

The contents of register rA is bitwise compared with the contents in register rB.

- rD is loaded with the position of the first matching byte pair, starting with MSB as position 1, and comparing until LSB as position 4
- If none of the byte pairs match, rD is set to 0

Pseudocode

```

if rB[0:7] = rA[0:7] then
  (rD) ← 1
else
  if rB[8:15] = rA[8:15] then
    (rD) ← 2
  else
    if rB[16:23] = rA[16:23] then
      (rD) ← 3
    else
      if rB[24:31] = rA[24:31] then
        (rD) ← 4
      else
        (rD) ← 0

```

Registers Altered

- rD

Latency

- 1 cycle

Note

This instruction is only available when the parameter C_USE_PCMP_INSTR is set to 1.

pcmpeq

Pattern Compare Equal

pcmpeq rD, rA, rB equality comparison with a positive boolean result

1 0 0 0 1 0	rD	rA	rB	1 0 0 0 0 0 0 0 0 0
0	6	1	1	2
		1	6	1
				3
				1

Description

The contents of register rA is compared with the contents in register rB.

- rD is loaded with 1 if they match, and 0 if not

Pseudocode

```
if (rB) = (rA) then
  (rD) ← 1
else
  (rD) ← 0
```

Registers Altered

- rD

Latency

- 1 cycle

Note

This instruction is only available when the parameter C_USE_PCMP_INSTR is set to 1.

pcmpne Pattern Compare Not Equal

pcmpne rD, rA, rB equality comparison with a negative boolean result

1	0	0	0	1	1	rD	rA	rB	1	0	0	0	0	0	0	0	0	0	0
0						6	1	1	2										3
							1	6	1										1

Description

The contents of register rA is compared with the contents in register rB.

- rD is loaded with 0 if they match, and 1 if not

Pseudocode

```

if (rB) = (rA) then
    (rD) ← 0
else
    (rD) ← 1
    
```

Registers Altered

- rD

Latency

- 1 cycle

Note

This instruction is only available when the parameter C_USE_PCMP_INSTR is set to 1.

put

Put to fsl interface

<i>naput</i>	rA, FSLx	put data to FSL x <i>n</i> = non-blocking <i>a</i> = atomic
<i>tnaput</i>	FSLx	put data to FSL x test-only <i>n</i> = non-blocking <i>a</i> = atomic
<i>ncaput</i>	rA, FSLx	put control to FSL x <i>n</i> = non-blocking <i>a</i> = atomic
<i>tncaput</i>	FSLx	put control to FSL x test-only <i>n</i> = non-blocking <i>a</i> = atomic

0	0 1 1 0 1 1	6	0 0 0 0 0	11	rA	16	1 n c t a 0 0 0 0 0 0	28	FSLx	31
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Description

MicroBlaze will write the value from register rA to the FSLx interface.

The put instruction has 16 variants.

The blocking versions (when 'n' is '0') will stall MicroBlaze until there is space available in the FSL interface. The non-blocking versions will not stall MicroBlaze and will set carry to '0' if space was available and to '1' if no space was available.

All data put instructions (when 'c' is '0') will set the control bit to the FSL interface to '0' and all control put instructions (when 'c' is '1') will set the control bit to '1'.

The test versions (when 't' bit is '1') will be handled as the normal case, except that the write signal to the FSL link is not asserted (thus no source register is required).

Atomic versions (when 'a' bit is '1') are not interruptible. This means that a sequence of atomic FSL instructions can be grouped together without an interrupt breaking the program flow. However, note that exceptions may still occur.

When MicroBlaze is configured to use an MMU (`C_USE_MMU >= 1`) these instructions are privileged. This means that if these instructions are attempted in User Mode (`MSR[UM] = 1`) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    (FSLx) ← (rA)
    if (n = 1) then
        MSR[Carry] ← (FSLx Full bit)
    (FSLx Control bit) ← C

```

Registers Altered

- MSR[Carry]
- ESR[EC], in case a privileged instruction exception is generated

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

The blocking versions of this instruction will stall the pipeline of MicroBlaze until the instruction can be completed. Interrupts are served when the parameter C_USE_EXTENDED_FSL_INSTR is set to 1, and the instruction is not atomic.

Note

These instructions are only available when the MicroBlaze parameter C_FSL_LINKS is greater than 0.

The extended instructions (atomic versions) are only available when the MicroBlaze parameter C_USE_EXTENDED_FSL_INSTR is set to 1.

putd

Put to fsl interface dynamic

<i>naputd</i>	rA, rB	put data to FSL rB[28:31] <i>n</i> = non-blocking <i>a</i> = atomic
<i>tnaputd</i>	rB	put data to FSL rB[28:31] test-only <i>n</i> = non-blocking <i>a</i> = atomic
<i>ncaputd</i>	rA, rB	put control to FSL rB[28:31] <i>n</i> = non-blocking <i>a</i> = atomic
<i>tncaputd</i>	rB	put control to FSL rB[28:31] test-only <i>n</i> = non-blocking <i>a</i> = atomic

0	0 1 0 0 1 1	6	0 0 0 0 0	11	rA	16	rB	21	1 n c t a 0 0 0 0 0 0	31
---	-------------	---	-----------	----	----	----	----	----	-----------------------	----

Description

MicroBlaze will write the value from register rA to the FSL interface defined by the four least significant bits in rB.

The putd instruction has 16 variants.

The blocking versions (when 'n' is '0') will stall MicroBlaze until there is space available in the FSL interface. The non-blocking versions will not stall MicroBlaze and will set carry to '0' if space was available and to '1' if no space was available.

All data putd instructions (when 'c' is '0') will set the control bit to the FSL interface to '0' and all control putd instructions (when 'c' is '1') will set the control bit to '1'.

The test versions (when 't' bit is '1') will be handled as the normal case, except that the write signal to the FSL link is not asserted (thus no source register is required).

Atomic versions (when 'a' bit is '1') are not interruptible. This means that a sequence of atomic FSL instructions can be grouped together without an interrupt breaking the program flow. However, note that exceptions may still occur.

When MicroBlaze is configured to use an MMU (`C_USE_MMU >= 1`) these instructions are privileged. This means that if these instructions are attempted in User Mode (`MSR[UM] = 1`) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    (FSL rB[28:31]) ← (rA)
    if (n = 1) then
        MSR[Carry] ← (FSL rB[28:31] Full bit)
    (FSL rB[28:31] Control bit) ← C

```

Registers Altered

- MSR[Carry]
- ESR[EC], in case a privileged instruction exception is generated

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

The blocking versions of this instruction will stall the pipeline of MicroBlaze until the instruction can be completed. Interrupts are served unless the instruction is atomic, which ensures that the instruction cannot be interrupted.

Note

These instructions are only available when the MicroBlaze parameter C_FSL_LINKS is greater than 0 and the parameter C_USE_EXTENDED_FSL_INSTR is set to 1.

rsub

Arithmetic Reverse Subtract

rsub	rD, rA, rB	Subtract
rsubc	rD, rA, rB	Subtract with Carry
rsubk	rD, rA, rB	Subtract and Keep Carry
rsubkc	rD, rA, rB	Subtract with Carry and Keep Carry

0	0	0	K	C	1	rD	rA	rB	0	0	0	0	0	0	0	0	0	0	0
0						6	1	1	2										3
							1	6	1										1

Description

The contents of register rA is subtracted from the contents of register rB and the result is placed into register rD. Bit 3 of the instruction (labeled as K in the figure) is set to one for the mnemonic rsubk. Bit 4 of the instruction (labeled as C in the figure) is set to one for the mnemonic rsubc. Both bits are set to one for the mnemonic rsubkc.

When an rsub instruction has bit 3 set (rsubk, rsubkc), the carry flag will Keep its previous value regardless of the outcome of the execution of the instruction. If bit 3 is cleared (rsub, rsubc), then the carry flag will be affected by the execution of the instruction.

When bit 4 of the instruction is set to one (rsubc, rsubkc), the content of the carry flag (MSR[C]) affects the execution of the instruction. When bit 4 is cleared (rsub, rsubk), the content of the carry flag does not affect the execution of the instruction (providing a normal subtraction).

Pseudocode

```

if C = 0 then
  (rD) ← (rB) + (rA) + 1
else
  (rD) ← (rB) + (rA) + MSR[C]
if K = 0 then
  MSR[C] ← CarryOut

```

Registers Altered

- rD
- MSR[C]

Latency

- 1 cycle

Notes

In subtractions, Carry = $\overline{\text{Borrow}}$. When the Carry is set by a subtraction, it means that there is no Borrow, and when the Carry is cleared, it means that there is a Borrow.

rsubi

Arithmetic Reverse Subtract Immediate

rsubi	rD, rA, IMM	Subtract Immediate
rsubic	rD, rA, IMM	Subtract Immediate with Carry
rsubik	rD, rA, IMM	Subtract Immediate and Keep Carry
rsubikc	rD, rA, IMM	Subtract Immediate with Carry and Keep Carry

0 0 1 K C 1	rD	rA	IMM
0	6	1	3
		1	6
			1

Description

The contents of register rA is subtracted from the value of IMM, sign-extended to 32 bits, and the result is placed into register rD. Bit 3 of the instruction (labeled as K in the figure) is set to one for the mnemonic rsubik. Bit 4 of the instruction (labeled as C in the figure) is set to one for the mnemonic rsubic. Both bits are set to one for the mnemonic rsubikc.

When an rsubi instruction has bit 3 set (rsubik, rsubikc), the carry flag will Keep its previous value regardless of the outcome of the execution of the instruction. If bit 3 is cleared (rsubi, rsubic), then the carry flag will be affected by the execution of the instruction. When bit 4 of the instruction is set to one (rsubic, rsubikc), the content of the carry flag (MSR[C]) affects the execution of the instruction. When bit 4 is cleared (rsubi, rsubik), the content of the carry flag does not affect the execution of the instruction (providing a normal subtraction).

Pseudocode

```

if C = 0 then
    (rD) ← sext(IMM) +  $\overline{(rA)}$  + 1
else
    (rD) ← sext(IMM) +  $\overline{(rA)}$  + MSR[C]
if K = 0 then
    MSR[C] ← CarryOut
    
```

Registers Altered

- rD
- MSR[C]

Latency

- 1 cycle

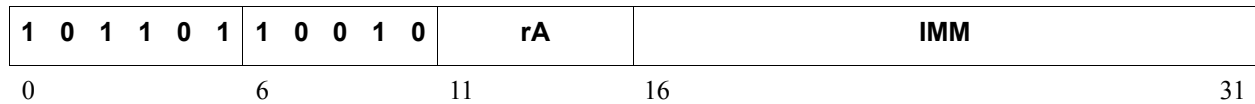
Notes

In subtractions, Carry = $\overline{(\text{Borrow})}$. When the Carry is set by a subtraction, it means that there is no Borrow, and when the Carry is cleared, it means that there is a Borrow. By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

rtbd

Return from Break

rtbd rA, IMM



Description

Return from break will branch to the location specified by the contents of rA plus the IMM field, sign-extended to 32 bits. It will also enable breaks after execution by clearing the BIP flag in the MSR.

This instruction always has a delay slot. The instruction following the RTBD is always executed before the branch target. That delay slot instruction has breaks disabled.

When MicroBlaze is configured to use an MMU ($C_USE_MMU \geq 1$) this instruction is privileged. This means that if the instruction is attempted in User Mode ($MSR[UM] = 1$) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    PC ← (rA) + sext(IMM)
    allow following instruction to complete execution
    MSR[BIP] ← 0
    MSR[UM] ← MSR[UMS]
    MSR[VM] ← MSR[VMS]

```

Registers Altered

- PC
- MSR[BIP], MSR[UM], MSR[VM]
- ESR[EC], in case a privileged instruction exception is generated

Latency

- 2 cycles

Note

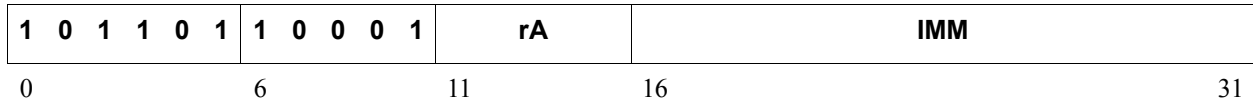
Convention is to use general purpose register r16 as rA.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

rtid

Return from Interrupt

rtid rA, IMM



Description

Return from interrupt will branch to the location specified by the contents of rA plus the IMM field, sign-extended to 32 bits. It will also enable interrupts after execution.

This instruction always has a delay slot. The instruction following the RTID is always executed before the branch target. That delay slot instruction has interrupts disabled.

When MicroBlaze is configured to use an MMU (C_USE_MMU >= 1) this instruction is privileged. This means that if the instruction is attempted in User Mode (MSR [UM] = 1) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    PC ← (rA) + sext(IMM)
    allow following instruction to complete execution
    MSR[IE] ← 1
    MSR[UM] ← MSR[UMS]
    MSR[VM] ← MSR[VMS]
    
```

Registers Altered

- PC
- MSR[IE], MSR[UM], MSR[VM]
- ESR[EC], in case a privileged instruction exception is generated

Latency

- 2 cycles

Note

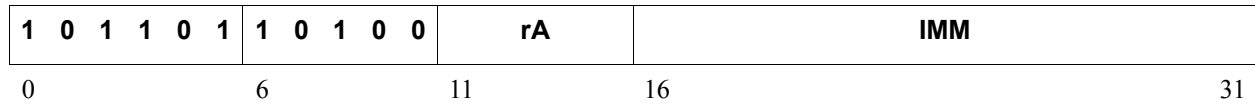
Convention is to use general purpose register r14 as rA.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

rted

Return from Exception

rted rA, IMM



Description

Return from exception will branch to the location specified by the contents of rA plus the IMM field, sign-extended to 32 bits. The instruction will also enable exceptions after execution.

This instruction always has a delay slot. The instruction following the RTED is always executed before the branch target.

When MicroBlaze is configured to use an MMU ($C_USE_MMU \geq 1$) this instruction is privileged. This means that if the instruction is attempted in User Mode ($MSR[UM] = 1$) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    PC ← (rA) + sext(IMM)
    allow following instruction to complete execution
    MSR[EE] ← 1
    MSR[EIP] ← 0
    MSR[UM] ← MSR[UMS]
    MSR[VM] ← MSR[VMS]
    ESR ← 0

```

Registers Altered

- PC
- MSR[EE], MSR[EIP], MSR[UM], MSR[VM]
- ESR

Latency

- 2 cycles

Note

Convention is to use general purpose register r17 as rA. This instruction requires that one or more of the MicroBlaze parameters $C_*__EXCEPTION$ are set to 1.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

Note: Code returning from an exception must first check if MSR[DS] is set, and in that case return to the address in BTR.

rtsd

Return from Subroutine

rtsd rA, IMM

1	0	1	1	0	1	1	0	0	0	0	rA	IMM				
0						6			1			1				3
								1			6				1	

Description

Return from subroutine will branch to the location specified by the contents of rA plus the IMM field, sign-extended to 32 bits.

This instruction always has a delay slot. The instruction following the RTSD is always executed before the branch target.

Pseudocode

```
PC ← (rA) + sext(IMM)
allow following instruction to complete execution
```

Registers Altered

- PC

Latency

- 2 cycles

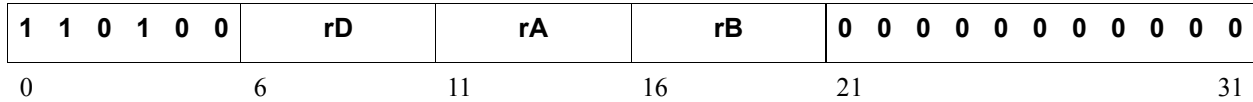
Note

Convention is to use general purpose register r15 as rA.

A delay slot must not be used by the following: imm, branch, or break instructions. Interrupts and external hardware breaks are deferred until after the delay slot branch has been completed.

sb**Store Byte**

sb rD, rA, rB

**Description**

Stores the contents of the least significant byte of register rD, into the memory location that results from adding the contents of registers rA and rB.

A data TLB miss exception occurs if virtual protected mode is enabled, and a valid translation entry corresponding to the address is not found in the TLB.

A data storage exception occurs if virtual protected mode is enabled, and access is prevented by no-access-allowed or read-only zone protection. No-access-allowed can only occur in user mode.

Pseudocode

```

Addr ← (rA) + (rB)
if TLB_Miss(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10010; ESR[S] ← 1
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Access_Protected(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10000; ESR[S] ← 1; ESR[DIZ] ← No-access-allowed
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else
    Mem(Addr) ← (rD) [24:31]

```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[UM], MSR[VM], MSR[UMS], MSR[VMS], if an exception is generated
- ESR[EC], ESR[S], if an exception is generated
- ESR[DIZ], if a data storage exception is generated

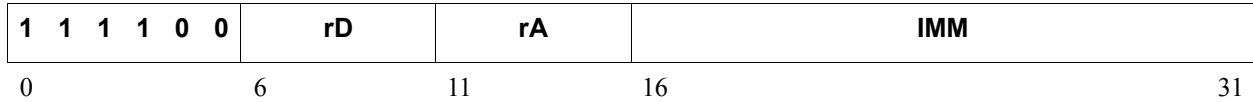
Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

sbi

Store Byte Immediate

sbi rD, rA, IMM



Description

Stores the contents of the least significant byte of register rD, into the memory location that results from adding the contents of register rA and the value IMM, sign-extended to 32 bits.

A data TLB miss exception occurs if virtual protected mode is enabled, and a valid translation entry corresponding to the address is not found in the TLB.

A data storage exception occurs if virtual protected mode is enabled, and access is prevented by no-access-allowed or read-only zone protection. No-access-allowed can only occur in user mode.

Pseudocode

```

Addr ← (rA) + sext (IMM)
if TLB_Miss (Addr) and MSR [VM] == 1 then
    ESR [EC] ← 10010; ESR [S] ← 1
    MSR [UMS] ← MSR [UM]; MSR [VMS] ← MSR [VM]; MSR [UM] ← 0; MSR [VM] ← 0
else if Access_Protected (Addr) and MSR [VM] == 1 then
    ESR [EC] ← 10000; ESR [S] ← 1; ESR [DIZ] ← No-access-allowed
    MSR [UMS] ← MSR [UM]; MSR [VMS] ← MSR [VM]; MSR [UM] ← 0; MSR [VM] ← 0
else
    Mem (Addr) ← (rD) [24:31]
    
```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[UM], MSR[VM], MSR[UMS], MSR[VMS], if an exception is generated
- ESR[EC], ESR[S], if an exception is generated
- ESR[DIZ], if a data storage exception is generated

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

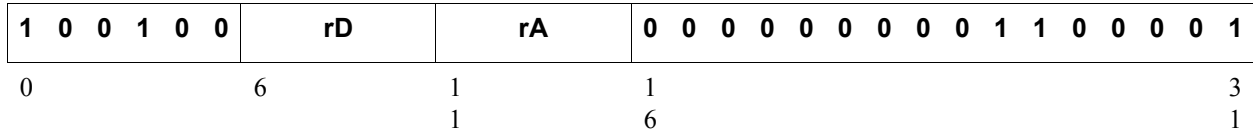
Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

sext16

Sign Extend Halfword

sext16 rD, rA



Description

This instruction sign-extends a halfword (16 bits) into a word (32 bits). Bit 16 in rA will be copied into bits 0-15 of rD. Bits 16-31 in rA will be copied into bits 16-31 of rD.

Pseudocode

```
(rD) [0:15] ← (rA) [16]
(rD) [16:31] ← (rA) [16:31]
```

Registers Altered

- rD

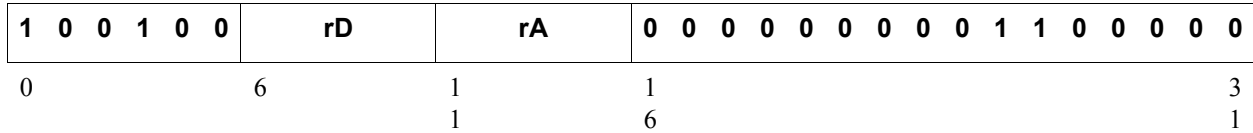
Latency

- 1 cycle

sext8

Sign Extend Byte

sext8 rD, rA



Description

This instruction sign-extends a byte (8 bits) into a word (32 bits). Bit 24 in rA will be copied into bits 0-23 of rD. Bits 24-31 in rA will be copied into bits 24-31 of rD.

Pseudocode

```
(rD) [0:23] ← (rA) [24]
(rD) [24:31] ← (rA) [24:31]
```

Registers Altered

- rD

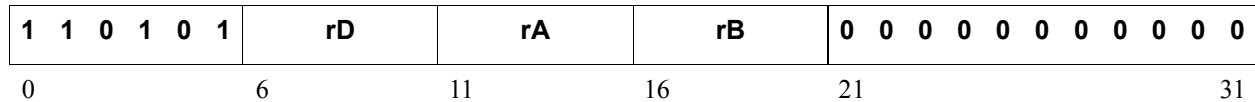
Latency

- 1 cycle

sh

Store Halfword

sh rD, rA, rB



Description

Stores the contents of the least significant halfword of register rD, into the halfword aligned memory location that results from adding the contents of registers rA and rB.

A data TLB miss exception occurs if virtual protected mode is enabled, and a valid translation entry corresponding to the address is not found in the TLB.

A data storage exception occurs if virtual protected mode is enabled, and access is prevented by no-access-allowed or read-only zone protection. No-access-allowed can only occur in user mode.

An unaligned data access exception occurs if the least significant bit in the address is not zero.

Pseudocode

```

Addr ← (rA) + (rB)
if TLB_Miss(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10010; ESR[S] ← 1
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Access_Protected(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10000; ESR[S] ← 1; ESR[DIZ] ← No-access-allowed
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Addr[31] != 0 then
    ESR[EC] ← 00001; ESR[W] ← 0; ESR[S] ← 1; ESR[Rx] ← rD
else
    Mem(Addr) ← (rD)[16:31]

```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[UM], MSR[VM], MSR[UMS], MSR[VMS], if a TLB miss exception or a data storage exception is generated
- ESR[EC], ESR[S], if an exception is generated
- ESR[DIZ], if a data storage exception is generated
- ESR[W], ESR[Rx], if an unaligned data access exception is generated

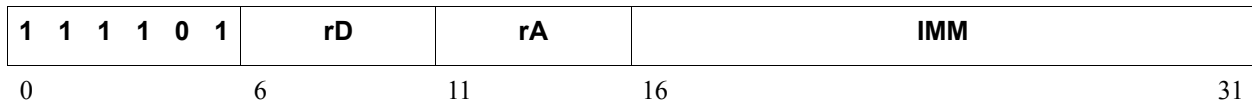
Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

shi

Store Halfword Immediate

shi rD, rA, IMM



Description

Stores the contents of the least significant halfword of register rD, into the halfword aligned memory location that results from adding the contents of register rA and the value IMM, sign-extended to 32 bits.

A data TLB miss exception occurs if virtual protected mode is enabled, and a valid translation entry corresponding to the address is not found in the TLB. A data storage exception occurs if virtual protected mode is enabled, and access is prevented by no-access-allowed or read-only zone protection. No-access-allowed can only occur in user mode. An unaligned data access exception occurs if the least significant bit in the address is not zero.

Pseudocode

```

Addr ← (rA) + sext(IMM)
if TLB_Miss(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10010; ESR[S] ← 1
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Access_Protected(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10000; ESR[S] ← 1; ESR[DIZ] ← No-access-allowed
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Addr[31] != 0 then
    ESR[EC] ← 00001; ESR[W] ← 0; ESR[S] ← 1; ESR[Rx] ← rD
else
    Mem(Addr) ← (rD)[16:31]
    
```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[UM], MSR[VM], MSR[UMS], MSR[VMS], if a TLB miss exception or a data storage exception is generated
- ESR[EC], ESR[S], if an exception is generated
- ESR[DIZ], if a data storage exception is generated
- ESR[W], ESR[Rx], if an unaligned data access exception is generated

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

sra

Shift Right Arithmetic

sra rD, rA

1	0	0	1	0	0	rD	rA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0						6	1	1														3
							1	6														1

Description

Shifts arithmetically the contents of register rA, one bit to the right, and places the result in rD. The most significant bit of rA (for example, the sign bit) placed in the most significant bit of rD. The least significant bit coming out of the shift chain is placed in the Carry flag.

Pseudocode

```
(rD)[0] ← (rA)[0]
(rD)[1:31] ← (rA)[0:30]
MSR[C] ← (rA)[31]
```

Registers Altered

- rD
- MSR[C]

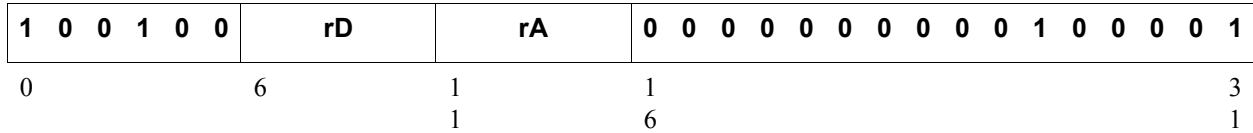
Latency

- 1 cycle

src

Shift Right with Carry

src rD, rA



Description

Shifts the contents of register rA, one bit to the right, and places the result in rD. The Carry flag is shifted in the shift chain and placed in the most significant bit of rD. The least significant bit coming out of the shift chain is placed in the Carry flag.

Pseudocode

```
(rD) [0] ← MSR [C]
(rD) [1:31] ← (rA) [0:30]
MSR [C] ← (rA) [31]
```

Registers Altered

- rD
- MSR[C]

Latency

- 1 cycle

srl

Shift Right Logical

srl rD, rA

1	0	0	1	0	0	rD	rA	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	
0						6	1	1																3
							1	6																1

Description

Shifts logically the contents of register rA, one bit to the right, and places the result in rD. A zero is shifted in the shift chain and placed in the most significant bit of rD. The least significant bit coming out of the shift chain is placed in the Carry flag.

Pseudocode

```
(rD) [0] ← 0
(rD) [1:31] ← (rA) [0:30]
MSR[C] ← (rA) [31]
```

Registers Altered

- rD
- MSR[C]

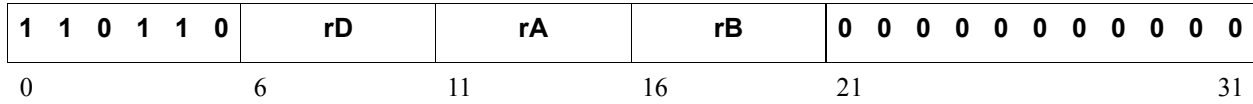
Latency

- 1 cycle

SW

Store Word

sw rD, rA, rB



Description

Stores the contents of register rD, into the word aligned memory location that results from adding the contents of registers rA and rB.

A data TLB miss exception occurs if virtual protected mode is enabled, and a valid translation entry corresponding to the address is not found in the TLB.

A data storage exception occurs if virtual protected mode is enabled, and access is prevented by no-access-allowed or read-only zone protection. No-access-allowed can only occur in user mode.

An unaligned data access exception occurs if the two least significant bits in the address are not zero.

Pseudocode

```

Addr ← (rA) + (rB)
if TLB_Miss(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10010; ESR[S] ← 1
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Access_Protected(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10000; ESR[S] ← 1; ESR[DIZ] ← No-access-allowed
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Addr[30:31] != 0 then
    ESR[EC] ← 00001; ESR[W] ← 1; ESR[S] ← 1; ESR[Rx] ← rD
else
    Mem(Addr) ← (rD) [0:31]
    
```

Registers Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[UM], MSR[VM], MSR[UMS], MSR[VMS], if a TLB miss exception or a data storage exception is generated
- ESR[EC], ESR[S], if an exception is generated
- ESR[DIZ], if a data storage exception is generated
- ESR[W], ESR[Rx], if an unaligned data access exception is generated

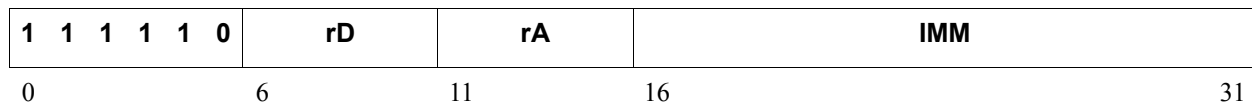
Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

swi

Store Word Immediate

swi rD, rA, IMM



Description

Stores the contents of register rD, into the word aligned memory location that results from adding the contents of registers rA and the value IMM, sign-extended to 32 bits.

A data TLB miss exception occurs if virtual protected mode is enabled, and a valid translation entry corresponding to the address is not found in the TLB.

A data storage exception occurs if virtual protected mode is enabled, and access is prevented by no-access-allowed or read-only zone protection. No-access-allowed can only occur in user mode.

An unaligned data access exception occurs if the two least significant bits in the address are not zero.

Pseudocode

```

Addr ← (rA) + sext(IMM)
if TLB_Miss(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10010; ESR[S] ← 1
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Access_Protected(Addr) and MSR[VM] == 1 then
    ESR[EC] ← 10000; ESR[S] ← 1; ESR[DIZ] ← No-access-allowed
    MSR[UMS] ← MSR[UM]; MSR[VMS] ← MSR[VM]; MSR[UM] ← 0; MSR[VM] ← 0
else if Addr[30:31] != 0 then
    ESR[EC] ← 00001; ESR[W] ← 1; ESR[S] ← 1; ESR[Rx] ← rD
else
    Mem(Addr) ← (rD)[0:31]

```

Register Altered

- rD, unless an exception is generated, in which case the register is unchanged
- MSR[UM], MSR[VM], MSR[UMS], MSR[VMS], if a TLB miss exception or a data storage exception is generated
- ESR[EC], ESR[S], if an exception is generated
- ESR[DIZ], if a data storage exception is generated
- ESR[W], ESR[Rx], if an unaligned data access exception is generated

Latency

- 1 cycle with C_AREA_OPTIMIZED=0
- 2 cycles with C_AREA_OPTIMIZED=1

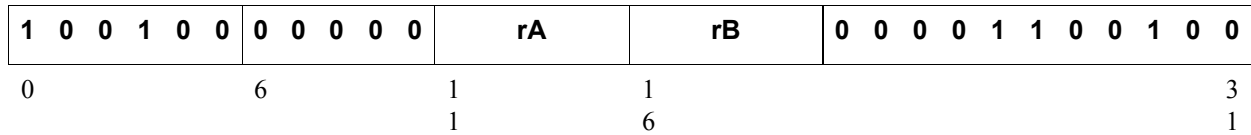
Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

wdc

Write to Data Cache

wdc rA,rB



Description

Write into the data cache tag to invalidate a cache line. The register rB value is not used. Register rA contains the address of the affected cache line.

The WDC instruction should only be used when the data cache is disabled (for example, MSR [DCE] = 0).

When MicroBlaze is configured to use an MMU (C_USE_MMU >= 1) this instruction is privileged. This means that if the instruction is attempted in User Mode (MSR [UM] = 1) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    if C_DCACHE_LINE_LEN = 4 then
        (DCache Line)[(Ra) >> 4].Tag ← 0
    if C_DCACHE_LINE_LEN = 8 then
        (DCache Line)[(Ra) >> 5].Tag ← 0
    
```

Registers Altered

- ESR[EC], in case a privileged instruction exception is generated

Latency

- 1 cycle

wic

Write to Instruction Cache

wic rA,rB

1	0	0	1	0	0	0	0	0	0	0	rA	rB	0	0	0	0	1	1	0	1	0	0	0
0						6					1	1										3	
											1	6										1	

Description

Write into the instruction cache tag to invalidate a cache line. The register rB value is not used. Register rA contains the address of the affected cache line.

The WIC instruction should only be used when the instruction cache is disabled (for example, MSR [ICE] = 0).

When MicroBlaze is configured to use an MMU (C_USE_MMU >= 1) this instruction is privileged. This means that if the instruction is attempted in User Mode (MSR [UM] = 1) a Privileged Instruction exception occurs.

Pseudocode

```

if MSR[UM] == 1 then
    ESR[EC] ← 00111
else
    if C_ICACHE_LINE_LEN = 4 then
        (ICache Line)[(Ra) >> 4].Tag ← 0
    if C_ICACHE_LINE_LEN = 8 then
        (ICache Line)[(Ra) >> 5].Tag ← 0

```

Registers Altered

- ESR[EC], in case a privileged instruction exception is generated

Latency

- 1 cycle

XOR

Logical Exclusive OR

xor rD, rA, rB

1 0 0 0 1 0	rD	rA	rB	0 0 0 0 0 0 0 0 0 0
0	6	1 1	1 6	2 1 3 1

Description

The contents of register rA are XORed with the contents of register rB; the result is placed into register rD.

Pseudocode

$$(rD) \leftarrow (rA) \oplus (rB)$$

Registers Altered

- rD

Latency

- 1 cycle

xori

Logical Exclusive OR with Immediate

xori rA, rD, IMM

1	0	1	0	1	0	rD	rA	IMM
0					6	1	1	3
						1	6	1

Description

The IMM field is extended to 32 bits by concatenating 16 0-bits on the left. The contents of register rA are XOR'ed with the extended IMM field; the result is placed into register rD.

Pseudocode

$$(rD) \leftarrow (rA) \oplus \text{sext}(IMM)$$

Registers Altered

- rD

Latency

- 1 cycle

Note

By default, Type B Instructions will take the 16-bit IMM field value and sign extend it to 32 bits to use as the immediate operand. This behavior can be overridden by preceding the Type B instruction with an imm instruction. See the instruction “imm,” page 147 for details on using 32-bit immediate values.

